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NASA-CR-170767

# ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

## PART III of IV: The Mosaic Transistor Array Applied to Custom Microprocessors PART IV of IV: Stored Logic Arrays - SLAs Implemented with Clocked CMOS



(NASA-CR-170767) ELECTRON LITHOGRAPHY STAR  
DESIGN GUIDELINES. PART 3: THE MOSAIC  
TRANSISTOR ARRAY APPLIED TO CUSTOM  
MICROPROCESSORS. PART 4: STORES LOGIC  
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**ENGINEERING & INDUSTRIAL RESEARCH STATION**

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### FINAL REPORT - PARTS III & IV

Submitted to:

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FINAL REPORT

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ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

Part 3: THE MOSAIC TRANSISTOR ARRAY APPLIED TO CUSTOM  
MICROPROCESSORS

Part 4: STORED LOGIC ARRAYS - SLAs IMPLEMENTED WITH  
CLOCKED CMOS

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August 31, 1982

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ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

Part 3: The Mosaic Transistor Array Applied  
to Custom Microprocessors

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J. Donald Trotter

THE MOSAIC TRANSISTOR ARRAY  
APPLIED TO  
CUSTOM MICROPROCESSORS

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# SUMMARY

The Mosaic Transistor Array is an extension of the STAR system developed by NASA which has dedicated field cells designed to be specifically used in semicustom microprocessor applications. The Sandia radiation hard bulk CMOS process is utilized in order to satisfy the requirements of space flights. A design philosophy is developed which utilizes the strengths and recognizes the weaknesses of the Sandia process. A style of circuitry is developed which incorporates the low power and high drive capability of CMOS. In addition the density achieved is better than that for classic CMOS, although not as good as for NMOS.

The basic logic functions for a data path are designed with compatible interface to the STAR grid system. In this manner either random logic or PLA type structures can be utilized for the control logic.

THE MOSAIC TRANSISTOR ARRAY  
APPLIED TO  
CUSTOM MICROPROCESSORS

I. Introduction

NASA at Marshall Space Flight Center has developed the Standard Transistor Array (STAR) as a means of providing quick turn-around to the design-fabrication cycle for custom integrated circuits. It is in essence a semicustom approach utilizing two levels of metal interconnect for customizing a chip to an application. It provides a means for fabrication of the diffused understructure at one location while the customizing double-layer metal can be applied at another. This allows organizations with proficiency in the thin film hybrid field to place the turn-around of custom I. C. development under their own control.

The associated STAR software allows for any mix of automatic layout and hand layout desired. Since the interconnections are regimented into a vertical-horizontal format, a reasonable display of the chip design can be mapped onto the column-row oriented line printer output. The STAR software system therefore does not demand an interactive graphics capability as a prerequisite for efficient operation.

Due to the double-layer metal aspect, STAR provides higher density than former automatic layout schemes which utilize only one layer of metal. The chip understructure is packed with transistors and the interconnections are handled overhead in the metal layers. The STAR scheme calls for all metal to be routed over a rigid grid structure. The interconnect points of the understructure transistors to the metalization layer, i.e., the grid points, are also fixed. The nature of the layout and fabrication of the understructure can be varied in all other aspects. Thus, the STAR approach can be suited to variations of technology. The intent is to separate the chip logic (in terms of interconnections of grid points) from the technology (in terms of solid state devices which feed through up to the grid). Logic, once defined, can easily be transferred from one technology to another or scaled up or down as desired. The understructure consists for the most part of two complementary transistors that are replicated over the whole

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chip. The task of changing technologies is reduced to redesigning two transistors. The accommodation within a technology to a specific vendor's desires on design rules can also be handled easily by redesigning the two transistors.

The STAR format dedicates certain of the horizontal and vertical lanes to the task of converting transistors into standard logic cell designs in order to ease the burden on automatic layout computation. This leaves clear lanes, plus unused cell lane segments, for the global interconnection of cells into the final chip design. STAR provides an excellent solution for custom integrated circuit needs in the area of random logic. There is a considerable need for such capability in the interfacing of a standard off-the-shelf microprocessors and their associated chips out to the real world. The STAR approach is not area efficient, however, in actual development of new microprocessors or similar chips.

The Mosaic Transistor Array (MTA), the subject of this research effort, is an approach aimed at reducing the turn-around time in the development of microprocessor or similar chips. Such chips tend to have segments devoted to RAM, ROM, PLA, and register activities. The STAR format, which is optimized for random logic, provides more interconnect lanes than are needed for these very regular structures. The MTA provides a small variety of understructures to accommodate each such activity. These understructures or field cells still maintain the same grid for compatibility with the random logic field cell, but the density of transistors may increase by a factor of four. The MTA loses the semicustom capability of the STAR. Prudent inclusion of extra random logic and/or PLA field cells into a design provides elbow room for mistakes or changes in control section. In concept one only has to revise the metal level masks. Wafers having the previous understructure processing would still be good for the new chip logic design.

A requirement for "total dose" radiation hardness constrains the design to be compatible with an available "hard" process. The Sandia silicon gate bulk CMOS process has been selected. This process presents interesting consequences for VLSI type designs. Channeling over the p-well is minimized by requiring the poly gate to extend over thin oxide into the P+ guard ring. This constraint compromises the normal CMOS circuit density -- much less compared with NMOS microprocessors.

The goal of this research project is to develop at least a first generation set of cells suitable for implementing the basic computer functions. In order to achieve flexibility for various applications, a customized control structure is visualized, possibly through microprogramming. In addition an organized approach to the

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assembly of the system building blocks from both circuit and topology points of view is required. A generalized data path (bit-slice) structure with a finite-state machine controller offers such an approach. Furthermore, the data flow through the bit-slice can be optimized for performance.

### 11. The Sandia CMOS Process with Double-Layer Metal

The Sandia process has been chosen since it represents a bulk silicon, radiation-hard process suitable for low-power space applications. Double layer metal add-on processing is assumed for this design -- just as in the case for the STAR program. The Sandia process is a p-well process with a separate P+ guard-ring diffusion. Consequently, the all N+ poly interconnection/gate layer is permitted to cross the field and p-well boundary. The fabrication steps required for n-type and p-type devices in the Sandia process are explained with the aid of a series of cross-sectional drawings in Figure 1.

The fabrication process begins with the growth of a thermal oxide on an n-type silicon wafer. Figure 1a shows the cross-section of the wafer after the thermal oxide has been grown. The next set of steps develops the p-well which is necessary for the isolation of the NMOS devices. In order to create the p-well, a hole must be made in the thermal oxide; this is done by a masking process. The p-well mask allows the thermal oxide to be removed in regions where a p-well is desired. The p-well is implanted and driven-in. A thin oxide is grown over the well in conjunction with the drive-in. The end result is indicated in Figure 1-b.

The P+ guard ring is the next addition. This guard ring serves to prevent the formation of a n-type channel over the lightly doped p-well -- even with the trapped positive charges in the oxide due to high doses of radiation. It also serves to inhibit SCR latch-up. The placement of the guard ring is controlled by a mask. Figure 1-c displays the wafer after a boron diffusion has produced the P+ guard ring. The guard ring mask (photoresist), indicated by the region enclosing the wavy lines, is shown in the figure.

A thick oxide, referred to as the field oxide, is then grown over the entire wafer. A mask is used to remove the thick oxide in regions where a thin oxide is desired. Figure 1-d illustrates the results.

The philosophy of the Sandia process is to have a thin oxide cover the entire p-well, including the guard ring and the PMOS devices. The other regions are covered by a thick oxide. It should be noted that the exposure to radiation creates hole-electron pairs in the oxide. The

electrons move relatively freely with moderate electric fields and are drained off by the positive potential interconnections. The holes are trapped at the oxide interface, resulting in an effective accumulation of positive charge which attracts electronic charge in the silicon below. The charge trapped is related to the oxide thickness to the second power, as a minimum. Consequently, over lightly-doped p-regions, only thin gate oxide is used in order to prevent channeling between "unrelated" N<sup>+</sup> nodes.

The thin oxide is provided by growing an oxide over the entire wafer. This oxide growth does not appreciably change the thickness of the thick oxide already present. A uniform polysilicon (poly) deposition follows the thin oxide growth. The poly is doped N<sup>+</sup> and will be used as the gates for all the transistors, both NMOS and PMOS. A mask referred to as the poly mask is used to remove the unwanted poly. The poly that remains is covered by growing a layer of thin oxide. Figure 1-e shows the cross-section of the wafer at this point in the fabrication process.

The wafer is now ready to be implanted with an N<sup>+</sup> material which will provide the sources and drains of all the NMOS devices. The N<sup>+</sup> implant mask (photoresist) is placed on the chip and the N<sup>+</sup> material implanted. The results from this N<sup>+</sup> implant step are indicated in Figure 1-f. The mask is still in place as indicated by wavy lines. It is obvious from the figure that the placement of the source and drain regions in the p-well for the NMOS devices is controlled by the implant mask and the poly. This provides a self-alignment of the NMOS transistors which is vital for proper operation of the device. One notes that a N<sup>+</sup> diffused region can be placed over the n-field in order to achieve ohmic contact to the n-substrate. The N<sup>+</sup> implant mask must fall within the thin-oxide region.

Similar to the NMOS devices, the PMOS devices are also self-aligned. The P<sup>+</sup> implant mask is used with a boron implant to dope the P<sup>+</sup> regions. Figure 1-g illustrates the results. From the figure it is seen that the placement of the source and drain regions of the PMOS devices is controlled by the thick oxide and the poly. The P<sup>+</sup> implant mask does not allow the P<sup>+</sup> material to be implanted inside the p-well except in regions for ohmic contact to the p-well.

The removal of the P<sup>+</sup> implant mask is followed by a glass coating. The cross-section of the wafer after this step appears as in Figure 1-h. It is seen in the figure that once the NMOS and PMOS devices have been constructed it remains only to provide the metal interconnections between devices.

As mentioned previously, double-layer metal processing is assumed. Before the first layer of metal is deposited on the chip, holes are cut into the glass that is present on the chip. This is done through another masking

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step; the mask in this case referred to as the contact mask. Figure 1-1 illustrates the chip after this masking step. The holes produced in the glass are called contacts, and the chip is ready for the first layer of metal.

The first layer of metal, sometimes a silicide, is deposited on the chip. A mask is used to remove the metal in locations where it is unwanted. This technique was used when the poly was laid on the chip and will be used again for the second layer of metal. After the first metal processing steps, the chip appears as in Figure 1-1. The metal is indicated in the figure by the cross-hatched area. In the figure the drain of the NMOS device has been connected to the drain of the PMOS device. Other connections between devices can be made by use of the metal.

The first metallization is followed by another glass coating similar to the glass coating step which followed the P+ implant. Before connections are made using the second metallization, holes are cut in the glass. Again a mask (called a via mask) is used. The resulting holes in the glass are known as vias. The cross-section of the chip after the vias have been etched is indicated in Figure 1-k.

The second layer of metal, appropriately referred to as top metal, is deposited on the chip. Once again a mask is used during the etching process to remove undesirable top metal. This second metallization step provides the remaining device connections that could not be completed with first metal. A final glass overcoat is placed on the chip as shown in Figure 1-1. The top metal has been cross-hatched opposite to that of first metal. According to the figure the connection of the gates of the NMOS and PMOS devices has been made by the top metal. This second metallization completes the process except for a pad mask step that allows terminal connections of the packaged chip to the integrated circuit.

The Sandia process can be quickly summarized by reviewing the different masks required during fabrication. Ten masks excluding the final pad mask comprise the complete set of required masks. These masks are in order: p-well, P+ guard ring, thin oxide, poly gate, N+ implant, P+ implant, contact, first metal, via, and second (top) metal.

The design rules used for the MTA project are the same as those developed for the radiation-hard STAR design. These rules are repeated in the following Table for the reader's convenience.

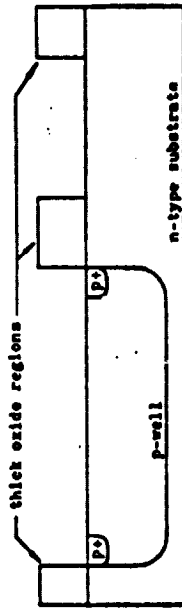


Figure 1d - Field Oxide on Chip

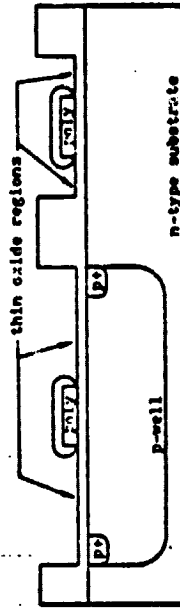


Figure 1e - Thin Oxide Growth and Poly Deposition

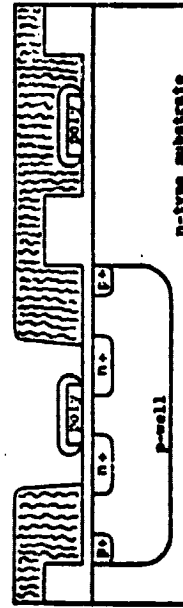


Figure 1f - Masking the n+ Implant Region

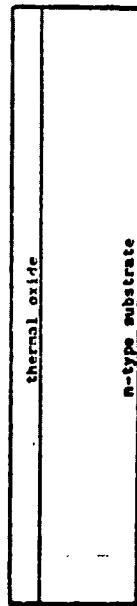


Figure 1a - Thermal Oxide on Wafer

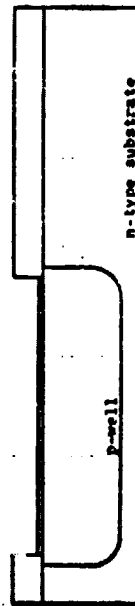


Figure 1b - Creating the p-well

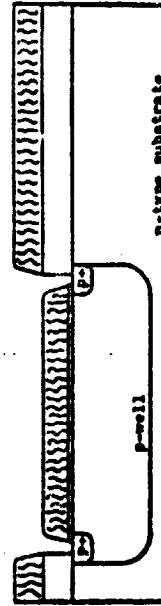
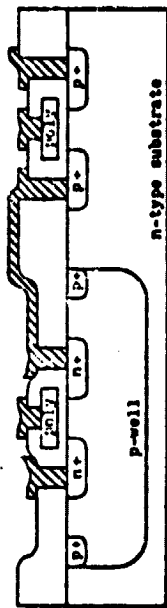
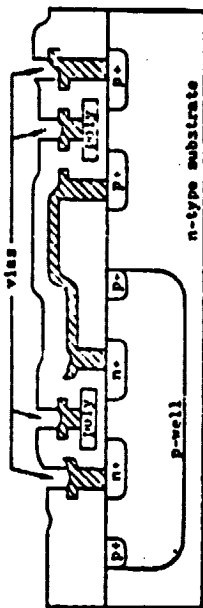


Figure 1c - Masking the p+ Guard Ring



### Figure 1j - First Metallization



### Figure 1k - Making Vias

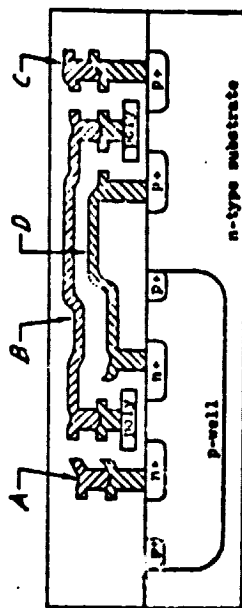


Figure 11 - Top Metal



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MASK	DESCRIPTION	NASA (MILS)	SANDIA (MICRONS)
LAYER 1:	P-WELL		
1.1.1	MINIMUM WIDTH	.2	5
1.1.2	MINIMUM SPACE	1.0	25
LAYER 2:	P+ GUARD-BAND		
2.2.1	MINIMUM WIDTH	.2	5
2.2.2	MINIMUM SPACE	.6	15
2.2.3	MINIMUM WIDTH AROUND WELL	.3	7
2.1.1	INSIDE EDGE OF GUARD BAND OVERLAP TO OUTSIDE OF P-WELL	0	0
LAYER 3:	THICK OXIDE (ALIGNED TO P+ GUARD-BAND)		
3.3.1	MINIMUM THICK OXIDE WIDTH	.3	7
3.3.2	MINIMUM THIN OXIDE SPACE	.3	8
3.3.3	MINIMUM SPACE (P+ TO P+)	.5	12
3.2.1	MINIMUM THIN OXIDE OVERLAP OF GUARD BAND EDGE	.2	5
3.2.2	MINIMUM THICK OXIDE TO GUARD BAND WHEN USED TO DEFINE N+	.325	8
3.2.3	MINIMUM THICK OXIDE TO GUARD BAND WHEN USED TO DEFINE P+ DRAIN	.65	17
3.2.4	SAME AS 3.2.3 EXCEPT P+ SOURCE	.5	13
3.1.1	MINIMUM THICK OXIDE TO P-WELL WHEN USED TO DEFINE P+ DRAIN	.85	21
3.1.2	SAME AS 3.1.1 EXCEPT P+ SOURCE	.675	17
3.3.3	MINIMUM THIN OXIDE TO SCRIBE LINE	2.0	50

Table Ia - NASA Design Rules For Sandia Process

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MASK	DESCRIPTION	NASA (MILS)	SANDIA (MICRONS)
LAYER 4:	POLY SILICON (ALIGNED TO THICK OXIDE)		
4.4.1	MINIMUM LINE	.25	6
4.4.2	MINIMUM SPACE	.25	6
4.4.2	MINIMUM PMOS GATE LENGTH	.25	5
4.4.3	MINIMUM NMOS GATE LENGTH	.2	8
4.3.1	MINIMUM POLY TO THICK OXIDE	.075	1
4.2.1	MINIMUM POLY TO GUARD BAND WHEN POLY DEFINES N+	.35	9
4.2.2	SAME AS 4.2.1 EXCEPT POLY DEFINES P+ DRAIN	.7	18
4.2.3	SAME AS 4.2.2 EXCEPT POLY DEFINES P+ SOURCE	.6	14
4.3.2	MINIMUM POLY GATE OVERLAP OF THICK OXIDE	.2	5
4.2.4	MINIMUM POLY OVERLAP OF GUARD RING	.25	6
4.1.1	MINIMUM POLY TO P-WELL WHEN POLY DEFINES P+ DRAIN	.9	22
4.1.2	SAME AS 4.1.1 EXCEPT POLY DEFINES P+ SOURCE	.7	18
LAYER 5:	N+ IMPLANT (ALIGNED TO THICK OXIDE)		
5.5.1	MINIMUM WIDTH	.2	5
5.5.2	MINIMUM SPACE	.2	6
5.2.1	MINIMUM N+ TO P+ GUARD	.4	10
LAYER 6:	P+ IMPLANT (ALIGNED TO THICK OXIDE)		
6.6.1	MINIMUM WIDTH	.2	5
6.6.2	MINIMUM SPACE	.5	12
6.2.1	MINIMUM P+ DRAIN TO P+ GUARD	.75	19
6.2.2	MINIMUM P+ SOURCE TO P+ GUARD @ VDD	.6	15
6.2.3	MINIMUM P+ DRAIN TO P+ GUARD @ VDD	.6	15
6.3.1	MINIMUM P+ TO THICK OXIDE WHICH DEFINES P+	.2	5
6.1.1	MINIMUM P+ TO P-WELL	.9	23
6.1.2	MINIMUM P+ TO P-WELL @ VDD	.75	19
6.5.1	MINIMUM P+ OVERLAP OF N+ FOR SHORTING	.05	1

Table 1b -(Continued). NASA Design Rules For Sandia Process

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MASK	DESCRIPTION	NASA (MILS)	SANDIA (MICRONS)
LAYER 7:	CONTACT (ALIGNED TO THICK OXIDE)		
7.7.1	MINIMUM CONTACT	.3 x .3	6 x 6
7.3.1	MINIMUM CONTACT INSIDE THICK OXIDE DIFFUSION	.2	11
7.4.1	MINIMUM CONTACT INSIDE POLY TO EDGE	.15	4
7.4.2	MINIMUM CONTACT OUTSIDE POLY TO EDGE	.2	
7.5.1	MINIMUM CONTACT INSIDE N+ DIFFUSION	.2	5
7.6.1	MINIMUM CONTACT INSIDE P+ DIFFUSION	.2	5
7.3.1	MINIMUM CONTACT FROM OXIDE STEP	.2	5
7.7.2	MINIMUM CONTACT FOR SHORT- ING OVERLAP DIFFUSIONS	.3	6
	MINIMUM P+ GUARD CONTACT	.3	7
LAYER 8:	METAL (ALIGNED TO CONTACT)		
8.8.1	MINIMUM METAL WIDTH	.5	8
8.8.2	MINIMUM METAL SPACE	.3	7
8.7.1	MINIMUM METAL CONTACT OVERLAP	.1	1
8.3.1	MINIMUM METAL TO SCRIBE LINE	2.0	50
LAYER 9:	VIA (ALIGNED TO FIRST METAL)		
9.9.1	MINIMUM VIA	.3 x .3	6 x 6
9.8.1	MINIMUM VIA INSIDE METAL	.1	1

Table Ic - (Continued). NASA Design Rules For Sandia Process

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MASK	DESCRIPTION	NASA (MILS)	SANDIA (MICRONS)
LAYER 10:	SECOND METAL (ALIGNED TO VIA)		
10.10.1	MINIMUM METAL WIDTH	.5	8
10.10.2	MINIMUM METAL SPACE	.3	7
10.9.1	MINIMUM METAL OVERLAP OF VIA	.1	1
10.3.1	MINIMUM BONDING PAD TO THIN OXIDE	1.5	40
10.10.3	MINIMUM BONDING PAD TO SECOND METAL	1.5	40
10.8.1	MINIMUM BONDING PAD TO FIRST METAL	1.5	40
10.10.4	MINIMUM UNBUFFERED PAD SPACING	8.5	220
10.10.5	MINIMUM BUFFERED PAD TO PAD SPACING	12.5	320
10.10.6	MINIMUM PAD SIZE	4 x 4	
10.10.7	MINIMUM VSS & VSS BUS WIDTH	.6	16
10.3.1	MINIMUM METAL TO SCRIBE LINE	2.0	50
10.11.1	PAD MASK INSIDE METAL PAD	.175	4

Table Id -(Continued). NASA Design Rules for Sandia Process

A generalized bit-slice structure with a finite-state machine controller is visualized to offer the flexibility objectives of this work. Mead and Conway suggest such an approach in their design text. However, their circuit philosophy is based on silicon gate NMOS with depletion devices -- a technology not suitable for the radiation environment of space flights. Their implementation of logic by means of register-to-register transfer paths through combination logic with each register being gated with a particular clock phase is not new; however, their extensive use of pass transistor logic to implement the combinational logic is unusual. Ratioed logic is principally restricted to the latches and registers; the ratioless pass transistor logic achieves the extended AND function at essentially zero stand-by power with the only performance compromise being fan-in. In this case the pass transistors are bi-lateral switches supplying current as a source-follower and sinking current as common source device. The source follower configuration has two short-comings:

- 1) Its final output value (pull-up) is limited by the body-effect to approximately 3.5 volts from a 5 volt supply -- even for a high performance NMOS process.
- 2) The time for the 0 to 3.5 volt transition is approximately five times longer than for the 3.5 to 0 volt transition (operating as a common source device).

Nevertheless, the simplicity of pass transistor logic is very attractive, particularly for VLSI designs. Precharging "high" can minimize transition delays in many cases.

Attempting to apply these concepts to CMOS technologies presents some interesting dilemmas. Replacing the ratioed inverters in the latches and registers by CMOS inverters is a straight-forward decision; however, the "structured" combinational logic poses a problem. Pass transistor switches, historically, in CMOS are implemented with pairs of devices, one NMOS and one PMOS for each switch, in order to avoid using a device in its compromised source-follower configuration. A bulk CMOS process with the NMOS devices built in a p-well, such as the Sandia process, provides NMOS devices with poor device characteristics compared with standard NMOS devices. The high p-well doping in the Sandia process (higher than normal for radiation hardness) produces a greater body-effect and reduced channel mobility compared with the standard. Consequently, the Sandia NMOS device is particularly unsuitable as a source-follower. As a result a direct implementation of the pass-transistor logic utilized by Mead and Conway is not practical in this design effort.

On the other hand classical CMOS is not practical for VLSI either. The CMOS device count for combinational logic is approximately twice that for NMOS. Further, implementing pass-transistor logic with classical CMOS requires true and complement signals to drive the NMOS and PMOS pair -- thus requiring roughly twice the number of control signals and drivers as for NMOS.

One alternative approach remains: implement pass-transistor logic with PMOS only, utilizing the fact that the PMOS devices in the Sandia process have a relatively low body-effect. In addition the P+ guard ring diffusion can be used as a diffusion tunnel under poly interconnections to provide a much needed cross-under capability.

Consider a CMOS latch with a PMOS pass-transistor serving as a multiplexing switch. The PMOS pass-gate will provide an output swing from about 1.5 volts to the power supply. Adjusting the ratio of the first inverter in the latch can provide the necessary level shifting. However, an additional NMOS device is required with the PMOS feedback transistor to supply the full voltage swing after "latch-up", thus providing the full gate drive signals, facilitating the full output drive from the inverters.

In this design philosophy the NMOS transistors, which require the extra area for channel stops, are utilized only where necessary. The NMOS device is an effective switch in the common-source configuration; however, a PMOS device is required for pull-up either in a classical CMOS fashion or precharged in a clocked scheme.

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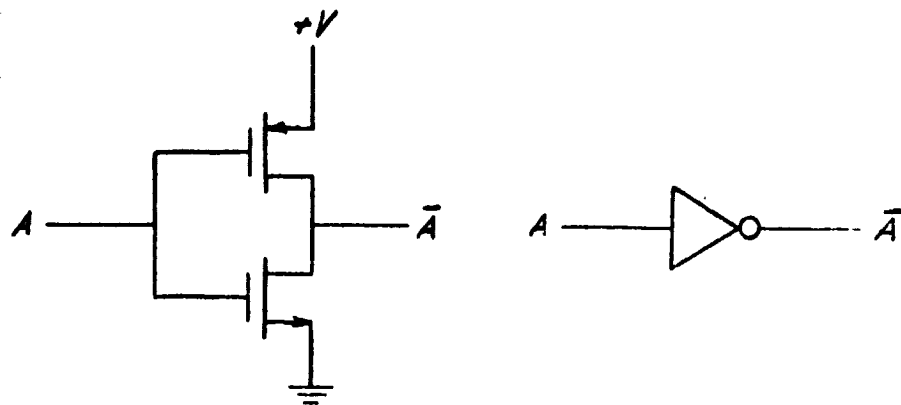


FIGURE 2a - CMOS INVERTER

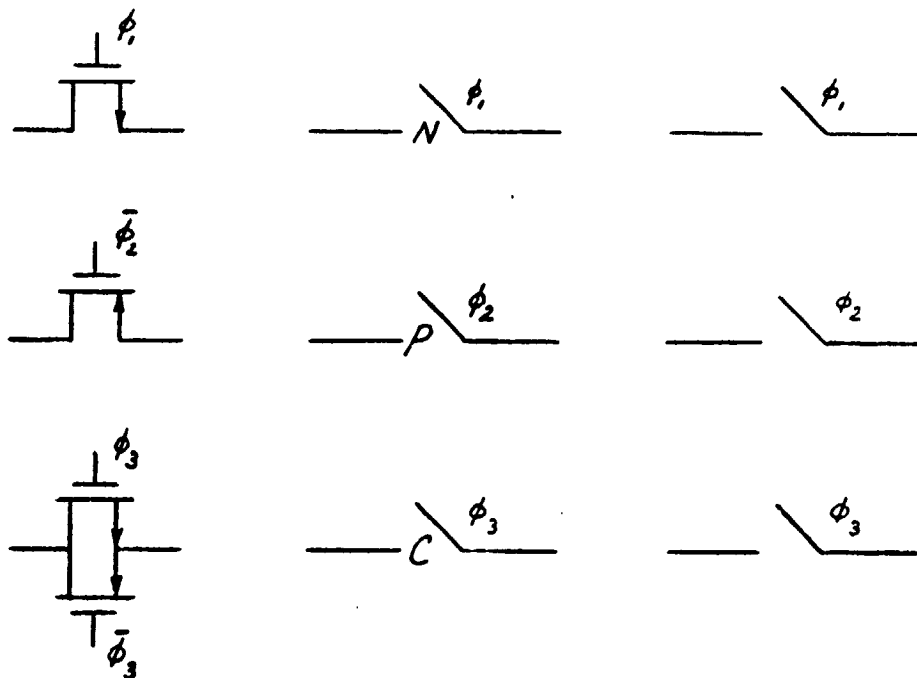


FIGURE 2b - THREE TYPES OF SWITCHES

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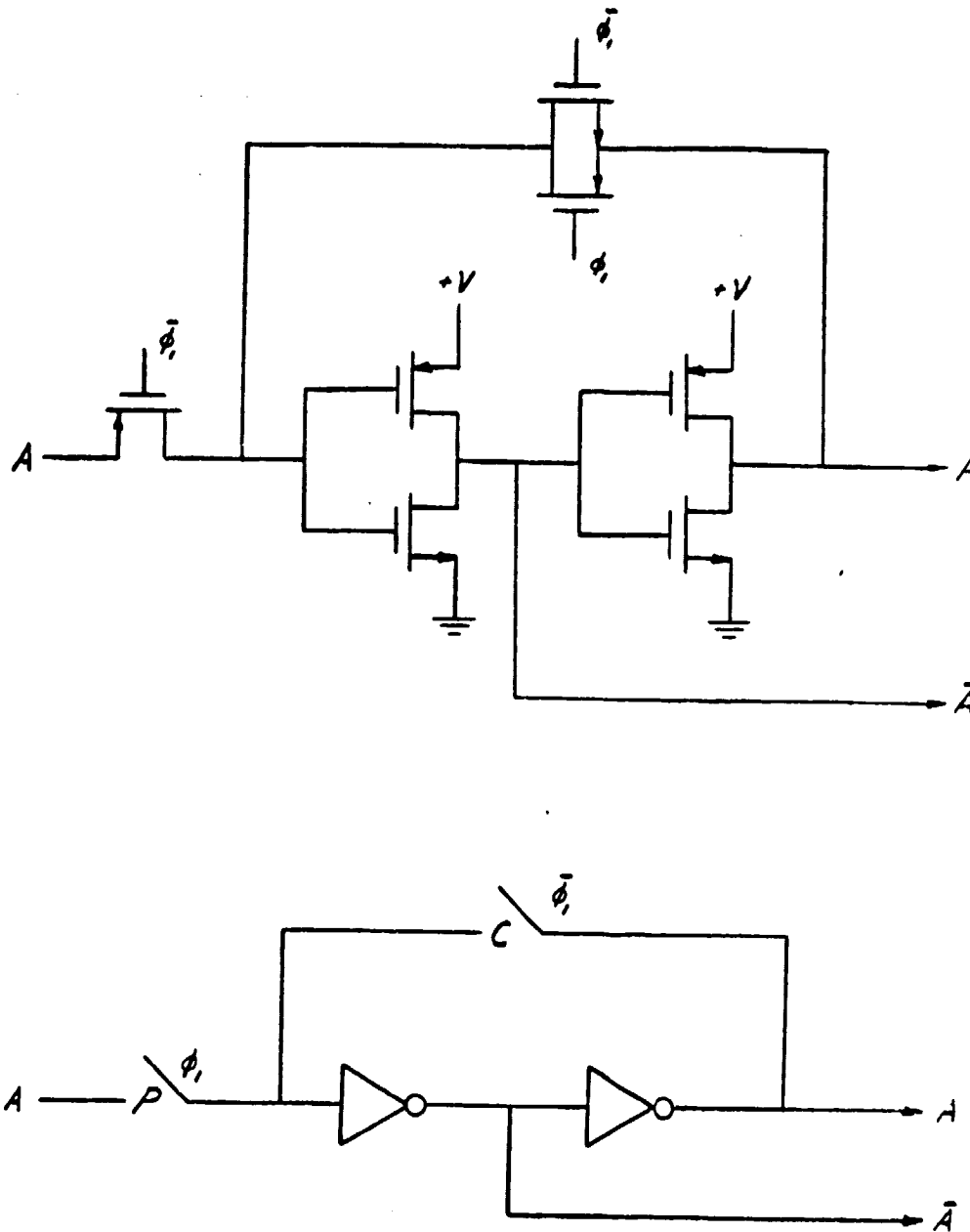


FIGURE 3 - A CMOS LATCH



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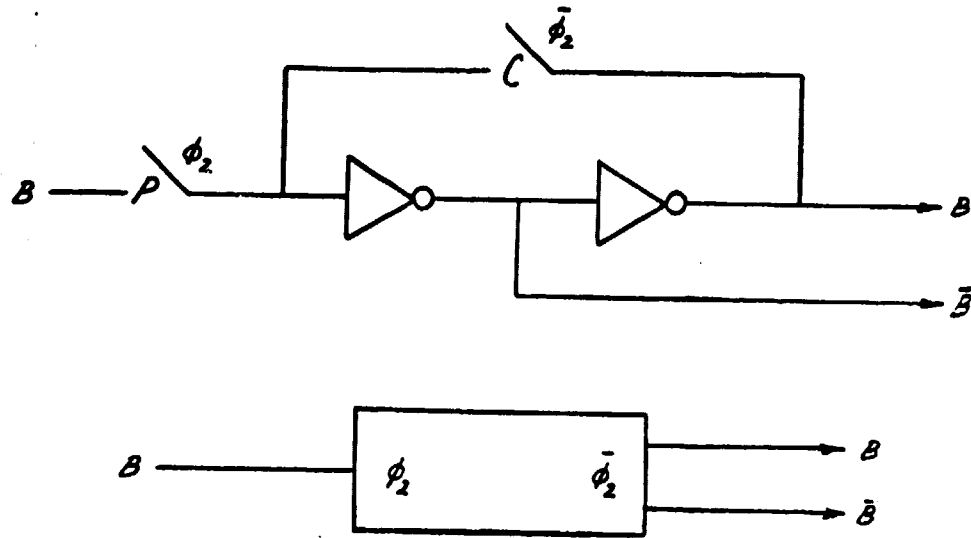


FIGURE 4 - BLOCK DIAGRAM OF A LATCH

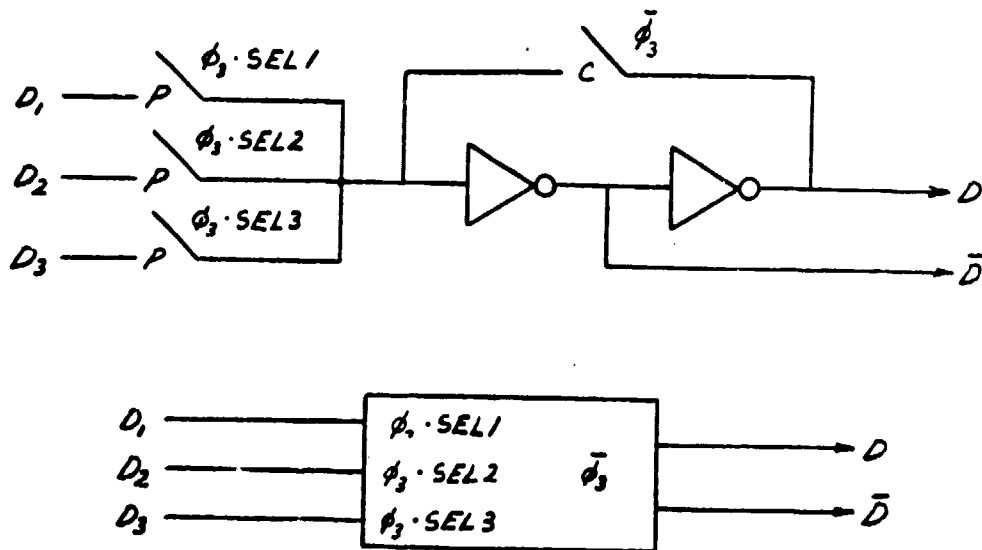


FIGURE 5 - LATCH WITH MULTIPLE INPUTS

### The Data Path Circuitry

Following the philosophy of Mead and Conway the data path is organised as parallel bit-slices from one port to another port as illustrated in Figure 6. Two different buses run between the two I/O ports and pass through the dual port register array, the barrel shifter, and the ALU. The ALU is built around a Manchester-type carry circuit. The carry-out signal is precharged high prior to logic evaluation (phase 2) and remains high unless the kill signal (K) is true or  $P \cdot \text{Cin}'$  is true where P is the pass signal and Cin' is complement of the carry-in signal.

$$\text{Cout}' = K + P \cdot \text{Cin}'$$

The kill and pass signals are generated by generalised function blocks, Figure 7. Each block contains four control signals and is driven by true and complement signals from two data sources, e.g.,

$$\text{Cout} = \text{C0} \cdot \text{A}' \cdot \text{B}' + \text{C1} \cdot \text{A}' \cdot \text{B} + \text{C2} \cdot \text{A} \cdot \text{B}' + \text{C3} \cdot \text{A} \cdot \text{B}$$

where A & B are data signals and C0 - C3 are control signals determined by the interpretation of the instruction.

The ALU is illustrated in Figure 8. The carry chain circuitry is implemented in NMOS since it is precharged high during phase 1 and conditionally discharged low during phase 2. The NMOS device is faster in this mode than the PMOS device. In addition the K and P function blocks can be precharged low during phase 1 and conditionally charged high during the evaluation of the logic, phase 2 -- thus achieving a ripple-through effect and saving one signal inversion and two logic gates.

The ALU is preconditioned for logic evaluation (precharged) during phase 1 and the logic is evaluated during phase 2. The data is transferred over the buses during phase 1 with the buses precharged low during phase 2. The two input latches, A and B, have multiplexing gates which select signals from three sources: 1) For latch A the possible signals are Bus A, the shifter output, and the shift-control signal. 2) For latch B the possible signals are Bus B, the shifter output, and the shift control signal. These signals are selected during phase 1 and latched during phase 2. The two output latches sample only the output of the R block during phase 2. Either output latch can drive either bus during phase 1.

The carry-chain output drives the carry input for the next bit-slice. After several bit-slices are added together, the discharge delay through the several pass-transistors can become excessively long. By utilising

the Cin signal generated to drive the R block as the drive signal for the carry propagation gate on a periodic basis, the pass-gate logic is buffered to minimize the carry propagation delay.

The data buses are precharged low during phase 2 and conditionally charged high through the enabled PMOS pass-gate as illustrated in Figure 12. The two port register cell with its PMOS drivers to either bus is shown in Figure 10.

Between the register and the ALU is a barrel shifter which concatenates the two buses with bus B being in the lower significant bit positions. With the shift constant equal to zero the shifter output corresponds to the A bus. With a non-zero shift constant, the output is shifted down the corresponding number of bits. The most significant bits from the A bus are omitted and the most significant bits of the B bus are included. Figure 11 illustrates the pass-gate logic used in a 4 x 4 bit barrel shifter. For the Sandia process the shifter is implemented in PMOS with the shift output precharged low in phase 2. If data is read out of a register to an input latch, the transfer occurs in phase 1 through three PMOS pass-gates: a dual port read switch, a shifter switch, and the multiplexer at the latch input.

The shifter also accomodates data transfers between bus A and a literal -port to the controller. The controller can supply a literal in phase 1. Data transfer in the reverse direction is possible in the opposite phase. Figure 13 illustrates the bi-lateral buffer.

A tri-state I/O buffer is given in Figures 14 and 15. The output is latched from either bus and enabled with an asynchronous signal with the latch driving either bus during phase 1. An appropriate number of inverter stages is included in the buffer to achieve the necessary capacitance driving capability.

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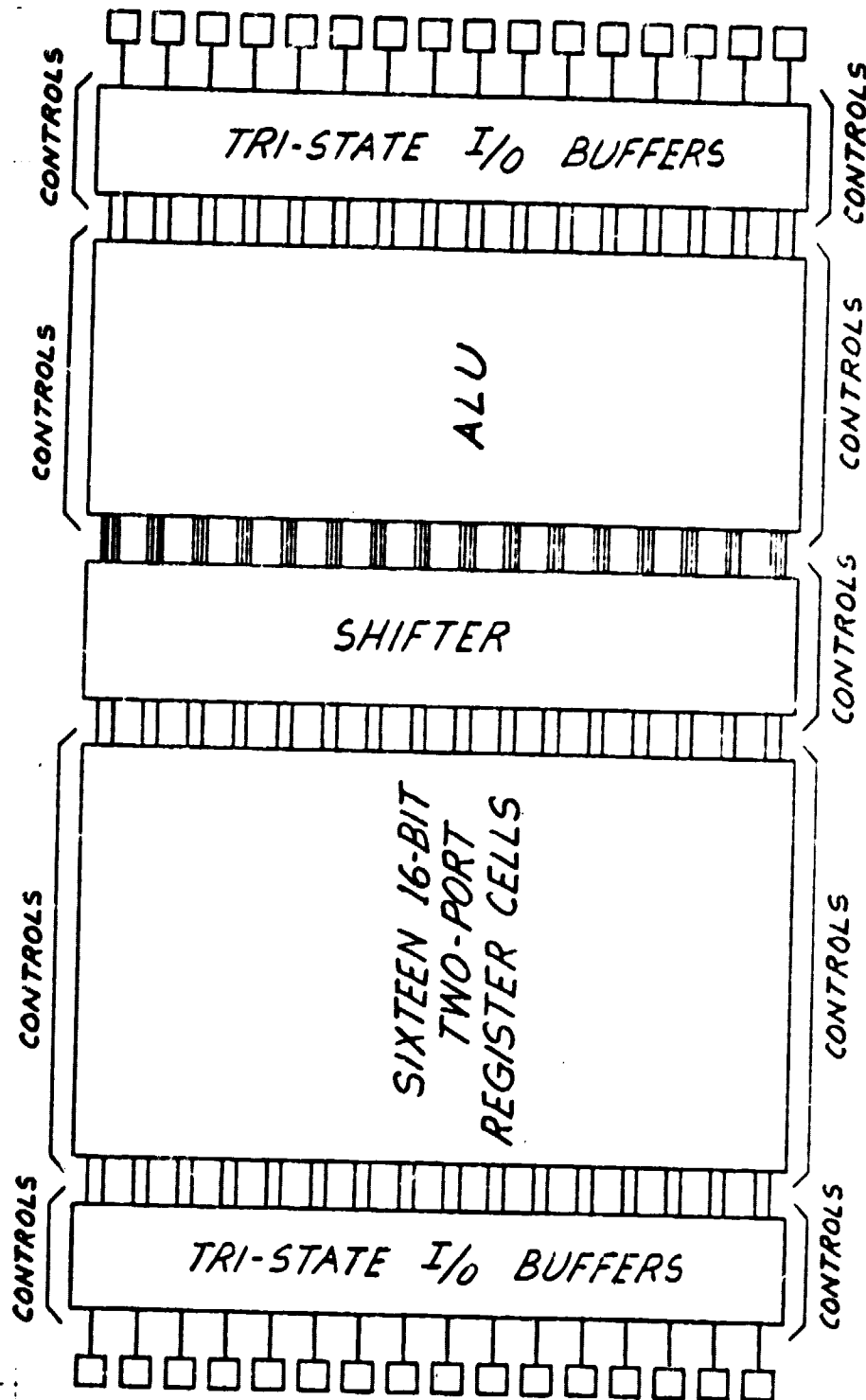


FIGURE 6 - CHIP PLAN FOR DATA PATH

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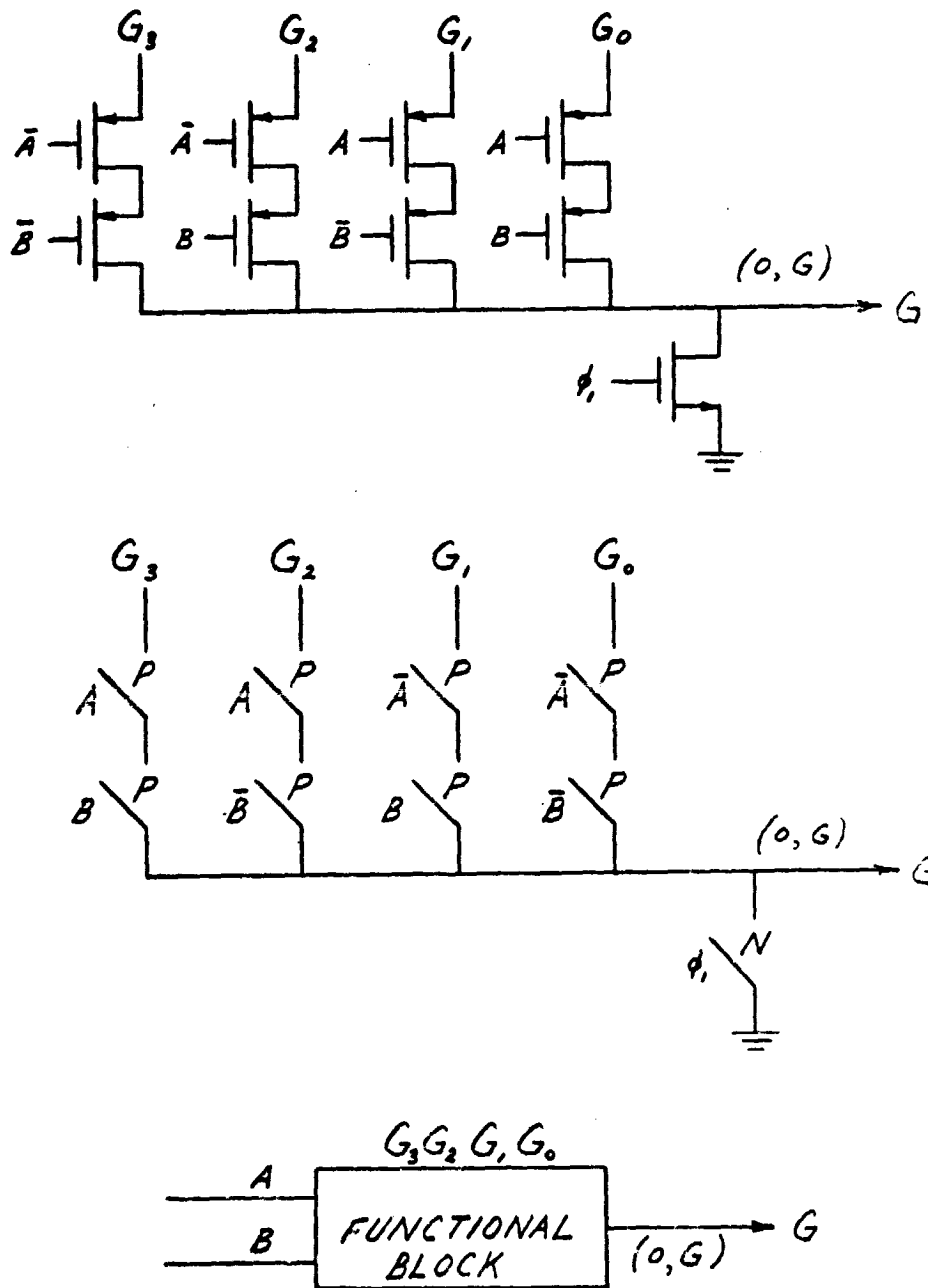


FIGURE 7 - GENERALIZED FUNCTIONAL BLOCK

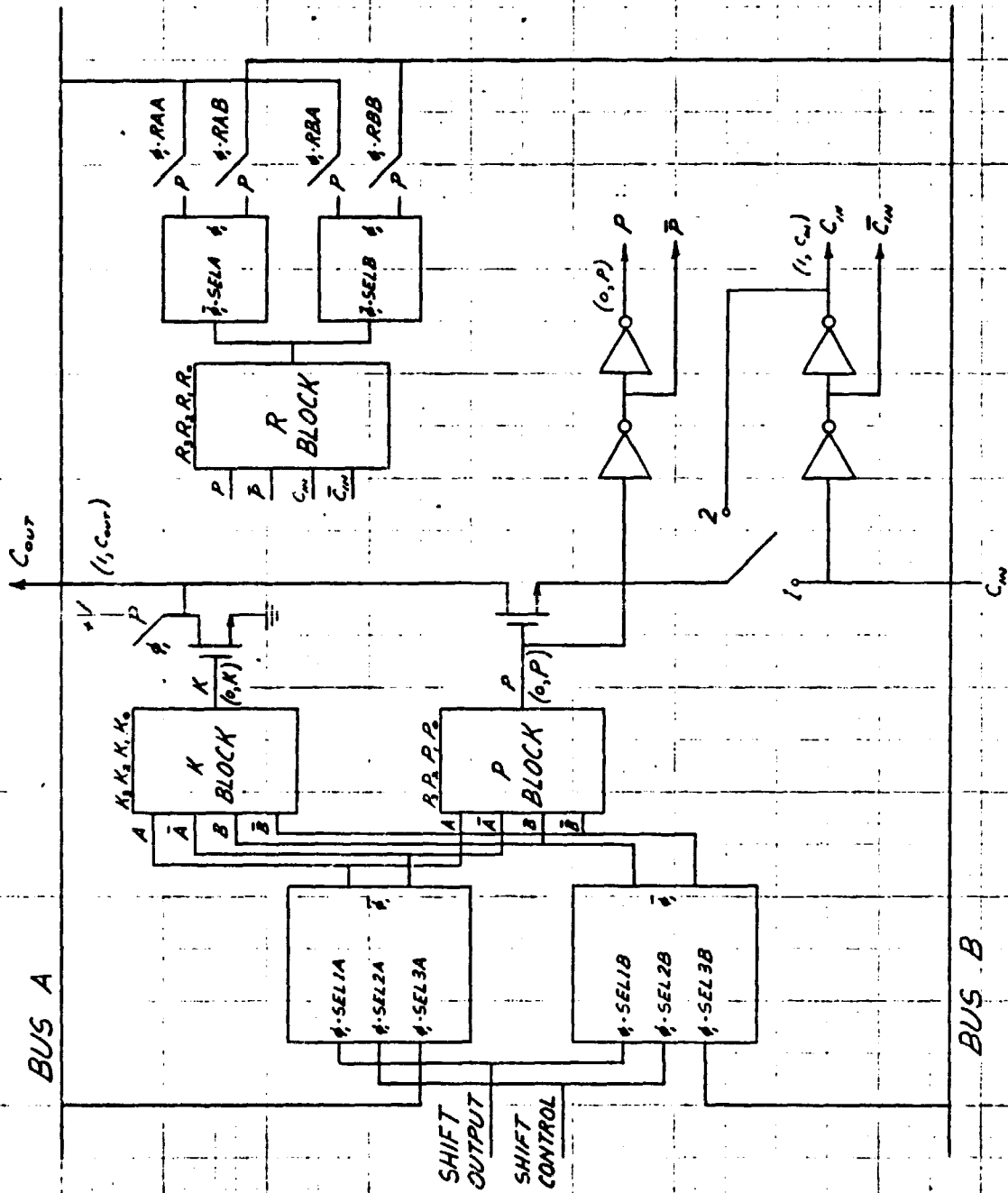


FIGURE 8 - A 1-BIT ARITHMETIC LOGIC UNIT  
TWO INPUT LATCHES, P AND K FUNCTIONAL BLOCKS, CARRY  
CHAIN, R FUNCTIONAL BLOCK, AND TWO OUTPUT LATCHES

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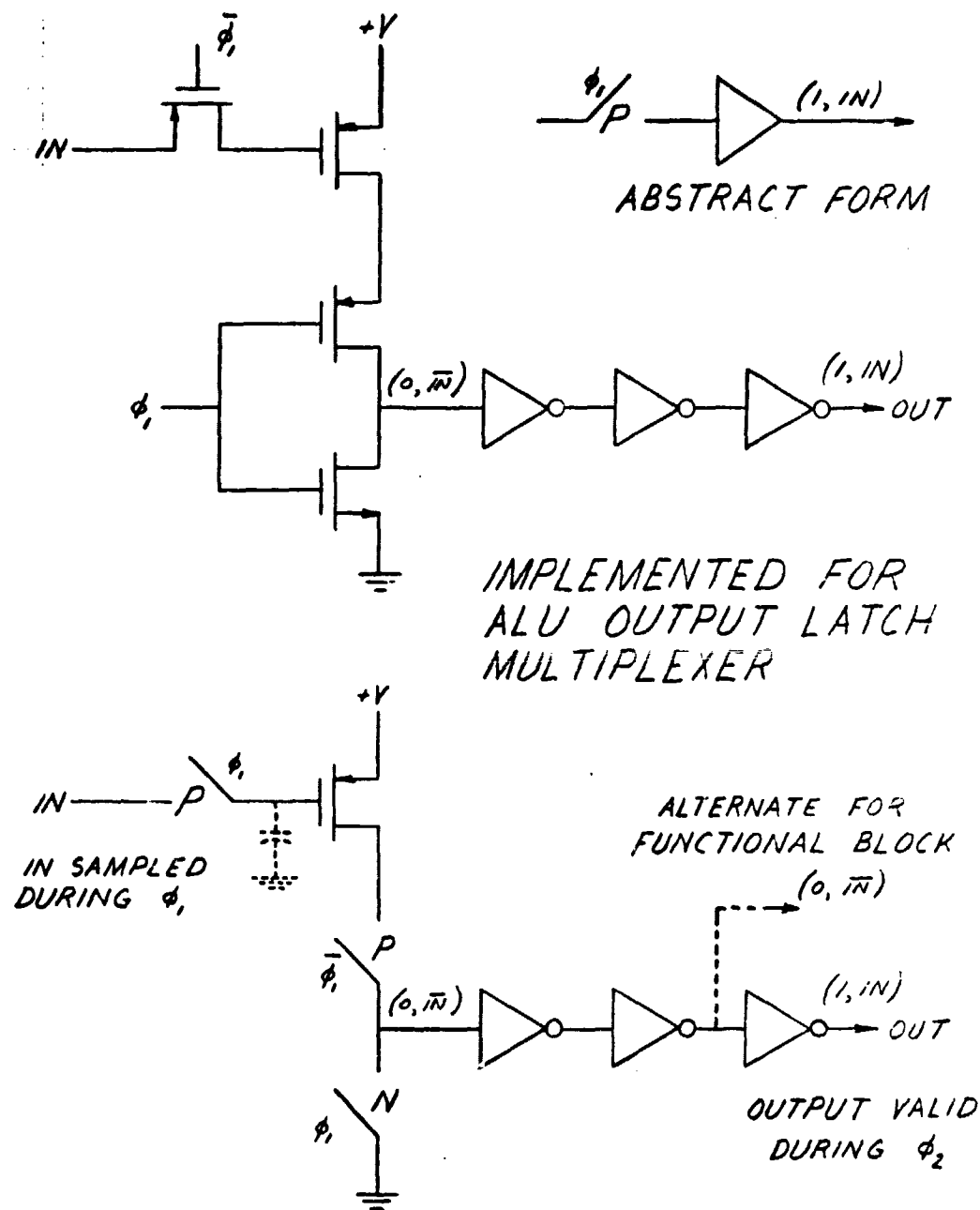


FIGURE 9 - CONTROL BUFFER

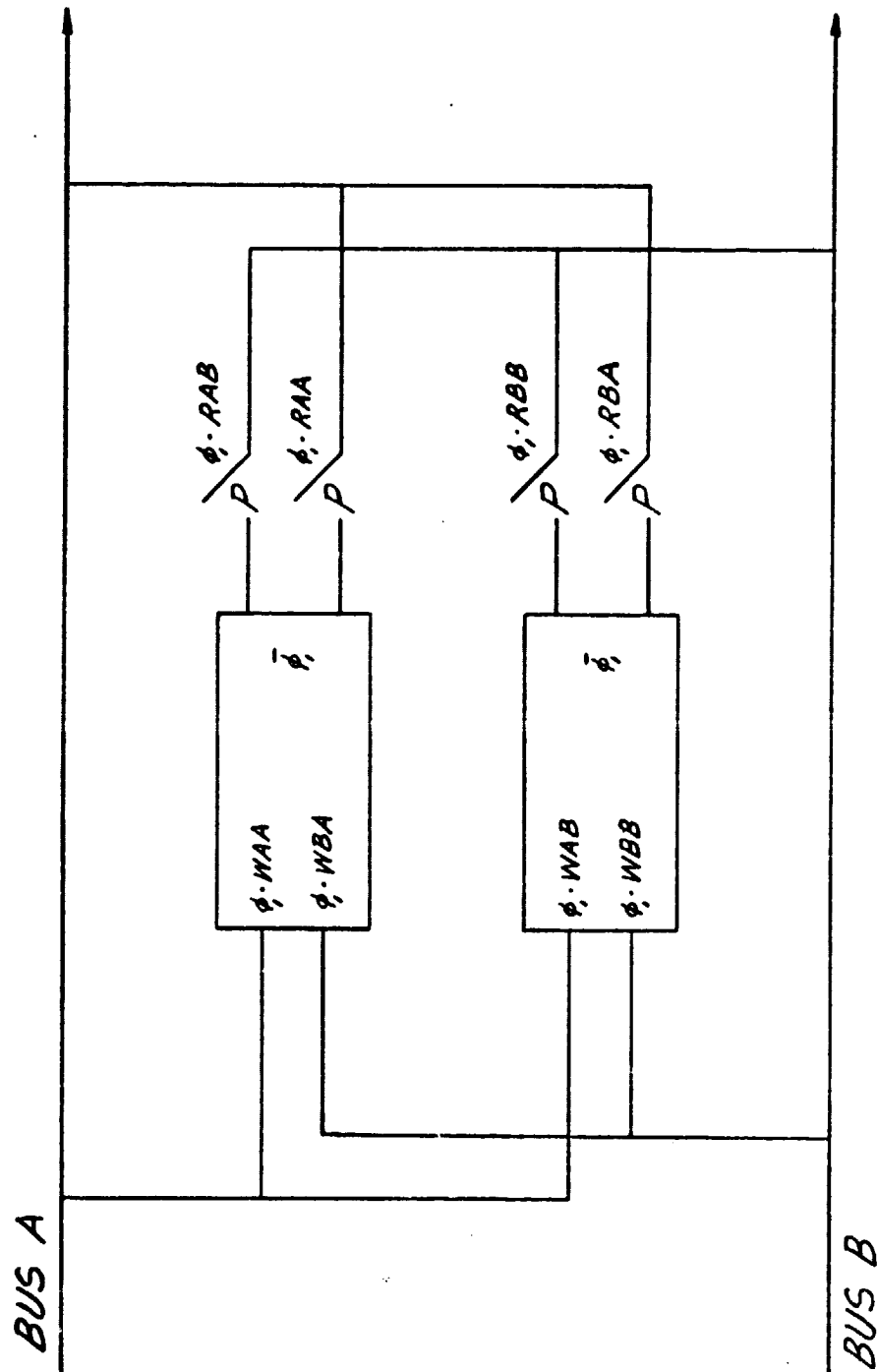


FIGURE 10 - TWO-PORT REGISTER CELL



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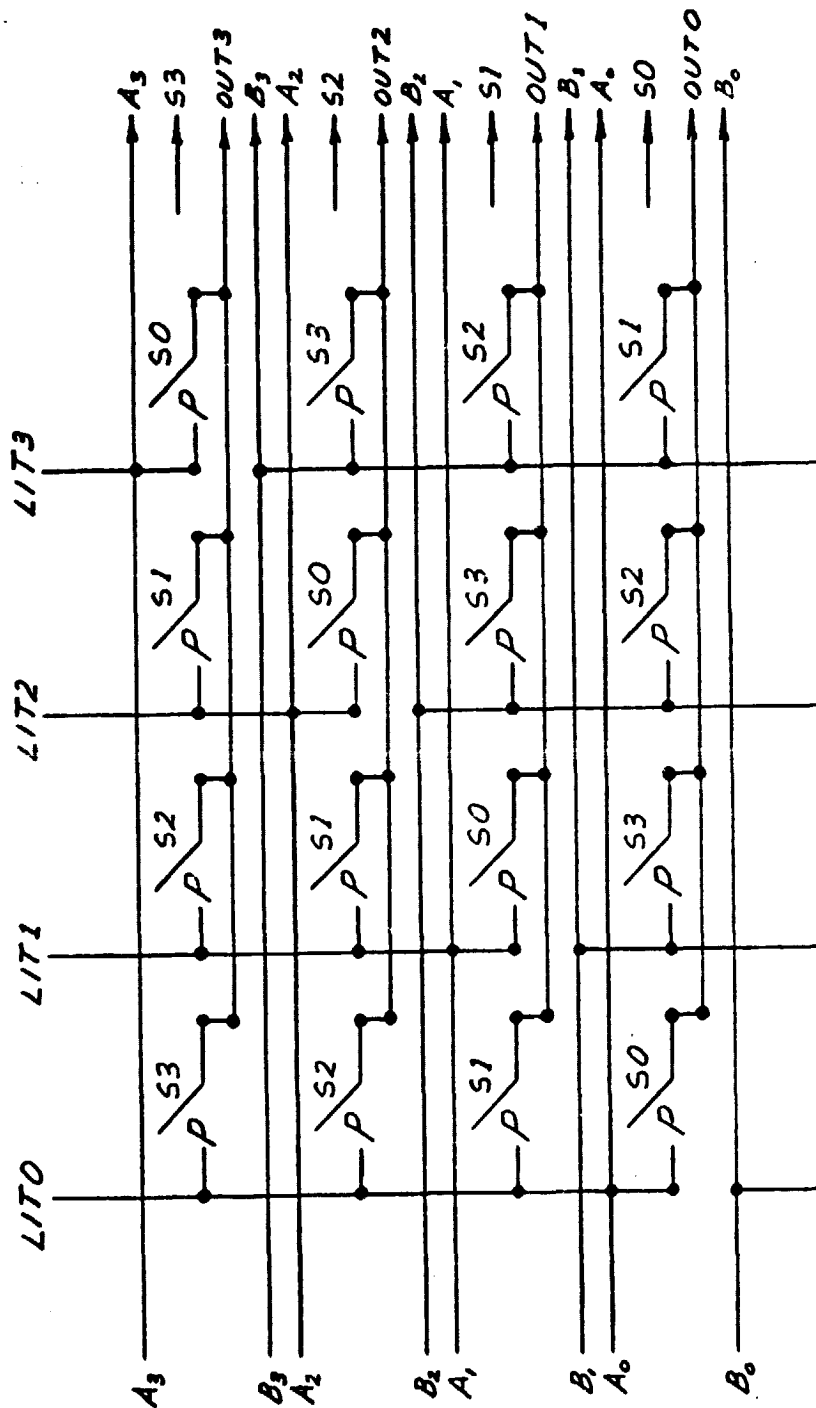
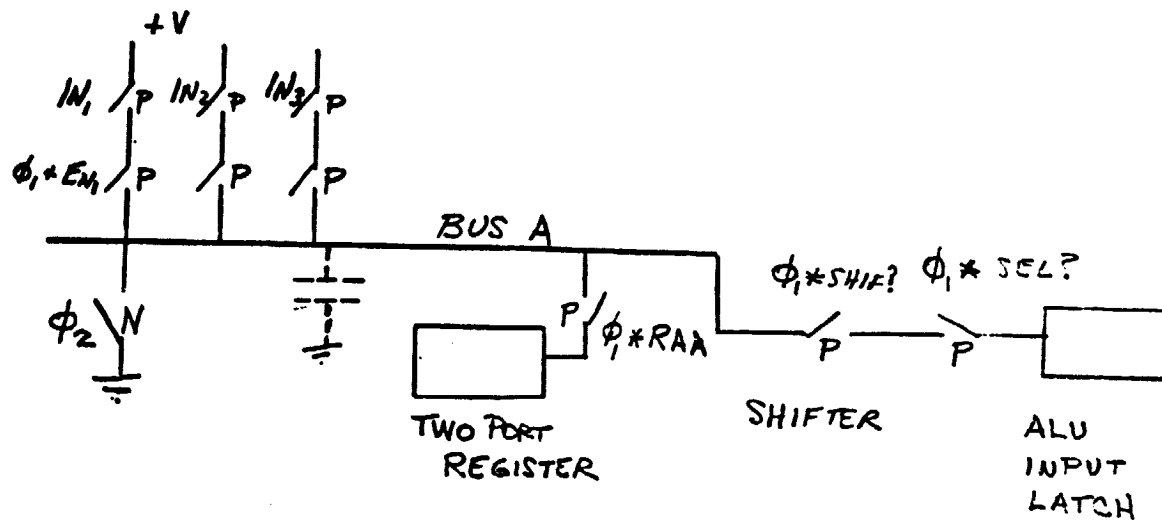


FIGURE 11 - A 4x4 BARREL SHIFTER

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- BUS DISCHARGED LOW IN  $\phi_2$
- BUS CONDITIONALLY CHARGED HIGH IN  $\phi_1$
- CONTROL BUFFERS
  - NON-INVERTING
  - SAMPLE INPUTS IN  $\phi_2$
  - OUTPUTS ARE PRECHARGED HIGH IN  $\phi_2$

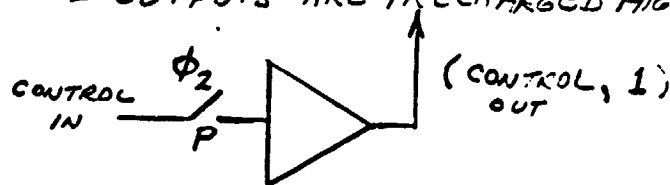


FIGURE 12 BUS CIRCUITRY AND TIMING

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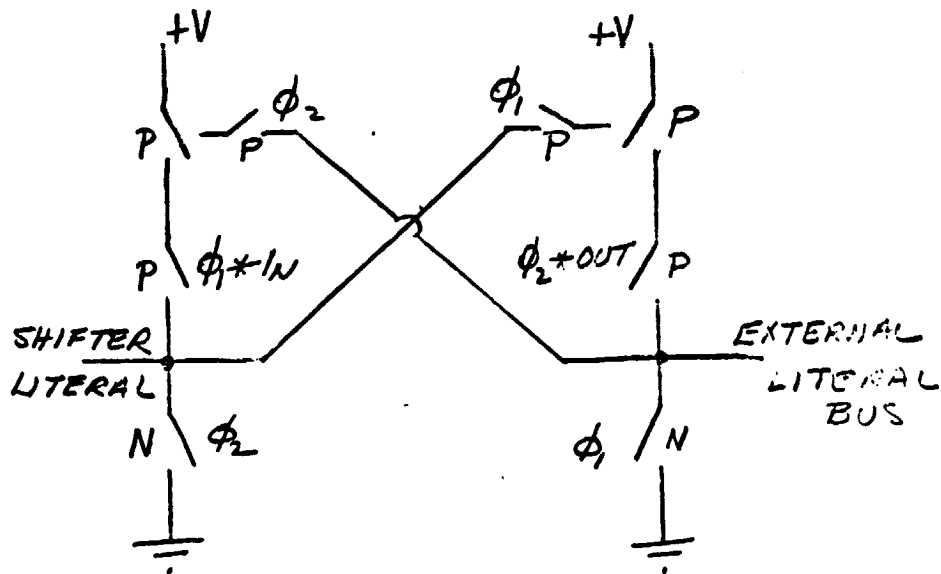
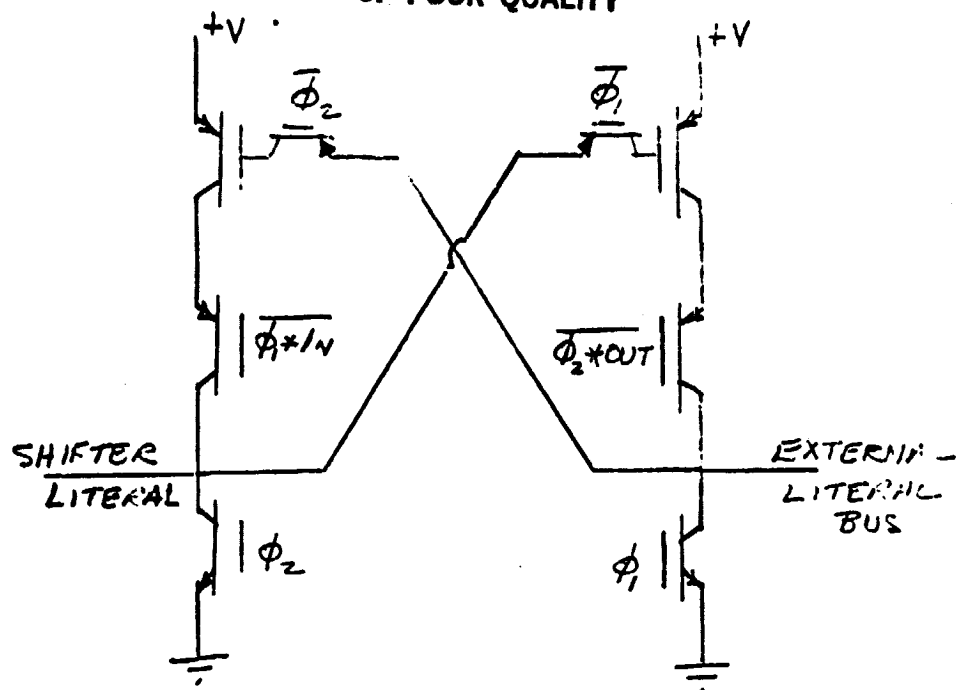


FIGURE 13 LITERAL BUFFER

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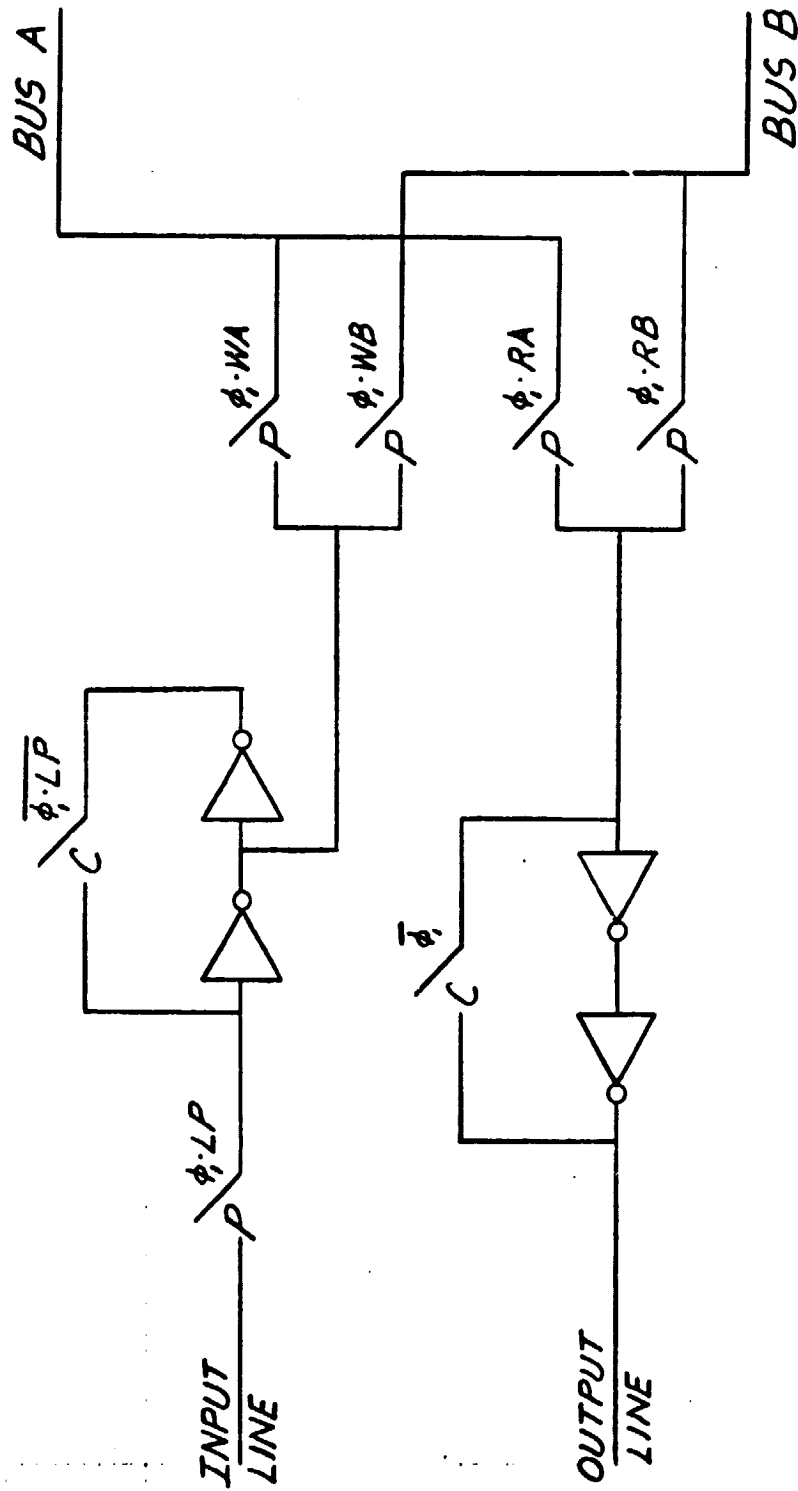


FIGURE 14 - INPUT/OUTPUT LATCH

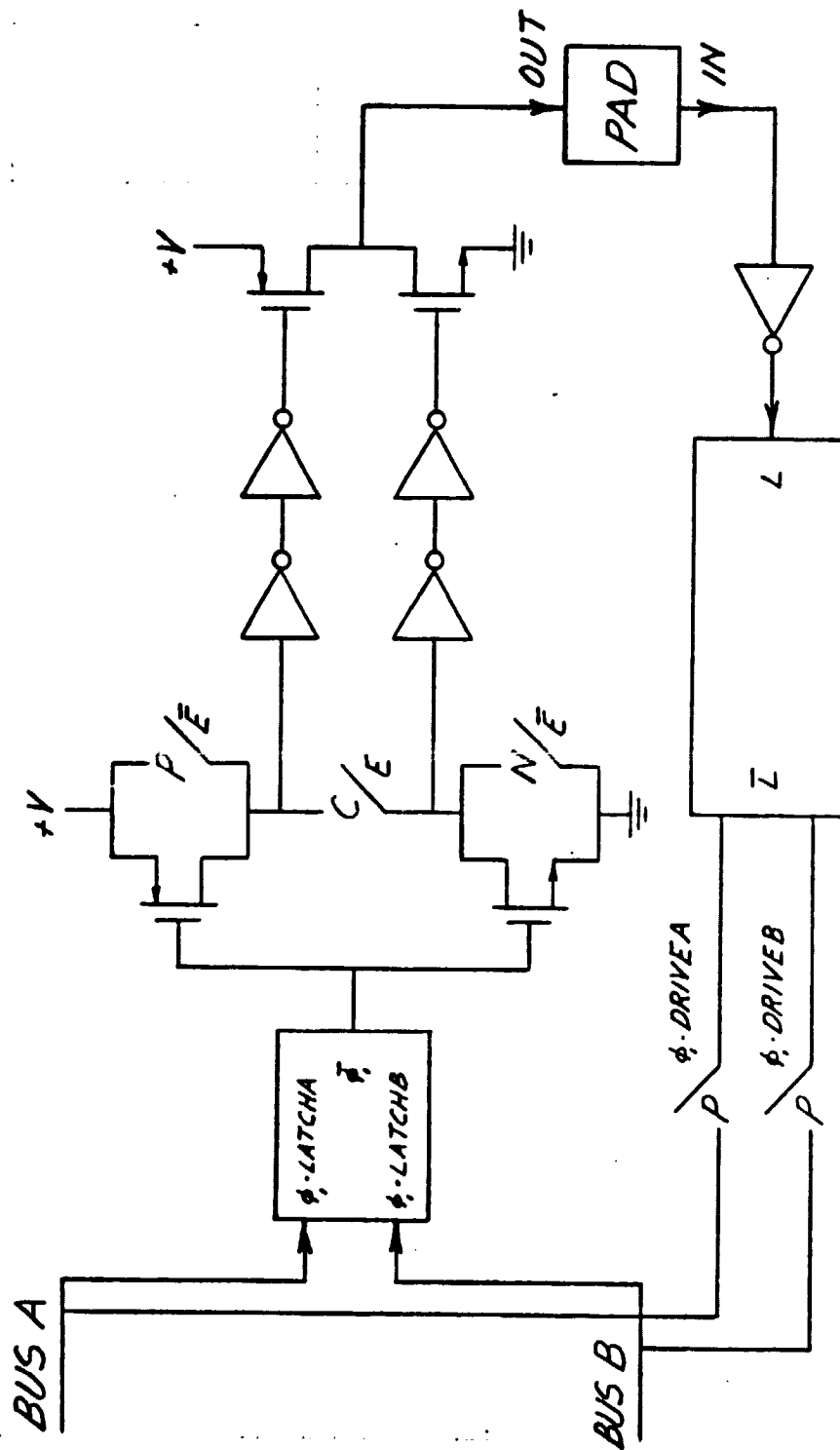


FIGURE 15 - TRI-STATE INPUT/OUTPUT BUFFER

#### V. Additional Comments

This design of the functional elements for a data path logic provides the foundation for implementing a microprocessor with the MTA concept. In this regard either the structured SLA described in another part of this report and/or conventional STAR cells can be used to implement the control logic.

The data path or bit-slice approach is quite flexible and is compatible with the concept of microprogramming with a PLA type structure. Electrically reprogrammable PLAs could even provide field changes in the basic instruction. The popularity of the bit-slice approach is exemplified by recent announcements from Hewlett-Packard and Bell Laboratories. It should also be noted that the Bellmac32 from Bell Laboratories is a 32 bit processor implemented with CMOS which uses their poly cell (standard cells) structures in conjunction with a data path function.

The detail drawings of the functional cells for the data path are provided in the appendix.

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REFERENCES

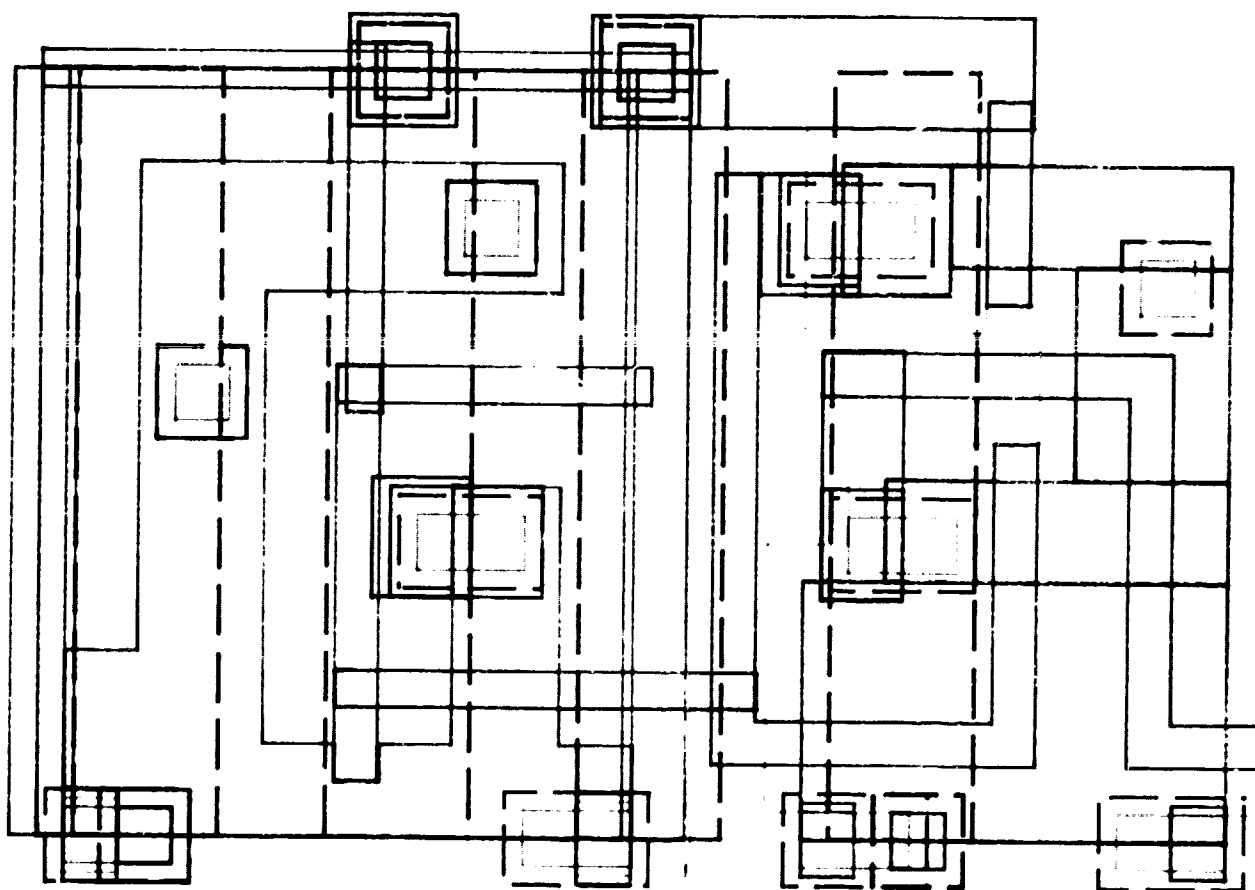
1. Carver Mead and Lynn Conway, Introduction to VLSI Systems,  
Addison-Wesley Publishing Company, 1980.

BASIC LATCH (no silicide)

1001

scale: 1001X

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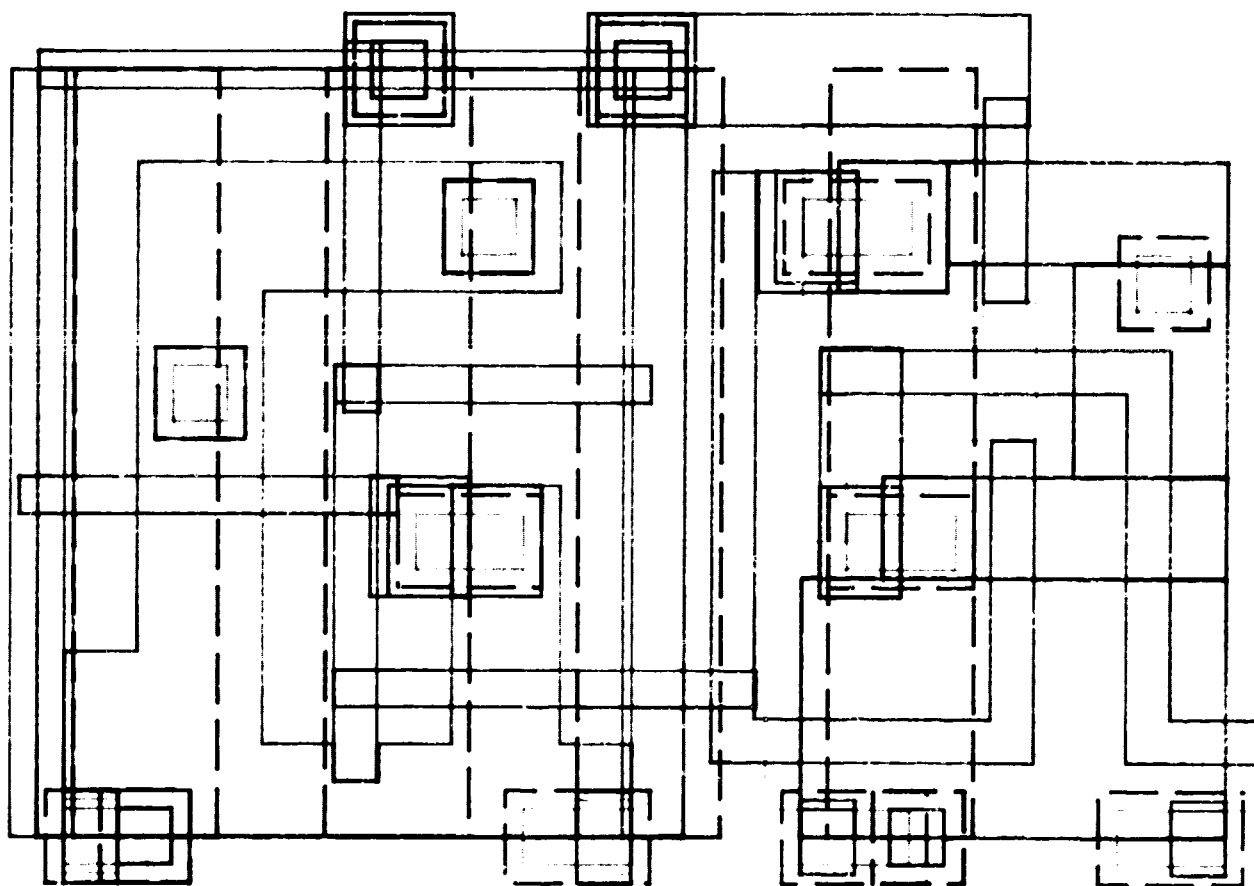


ODD LATCH ( gate added )

1002

scale: 1001X

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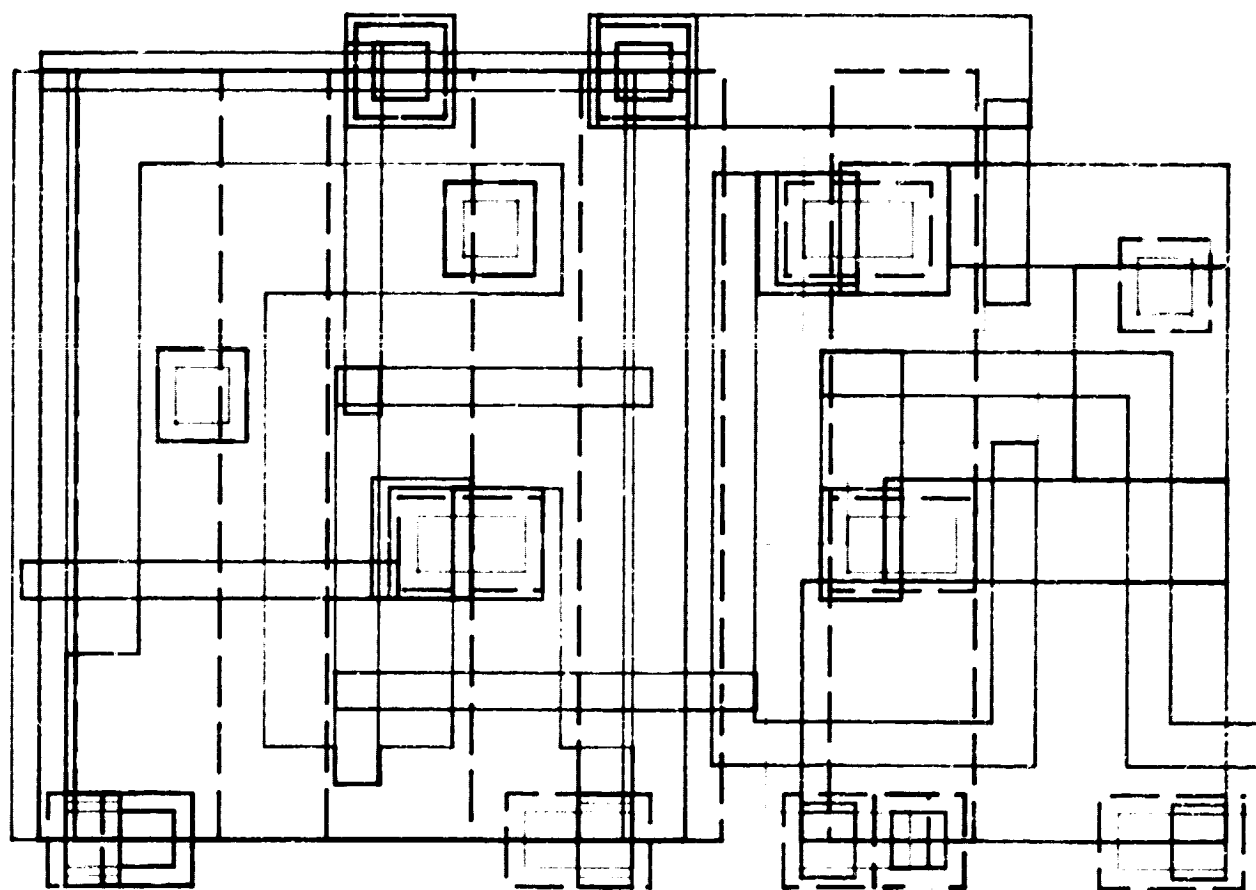
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EVEN LATCH (gate added )

1003

scale: 1001X

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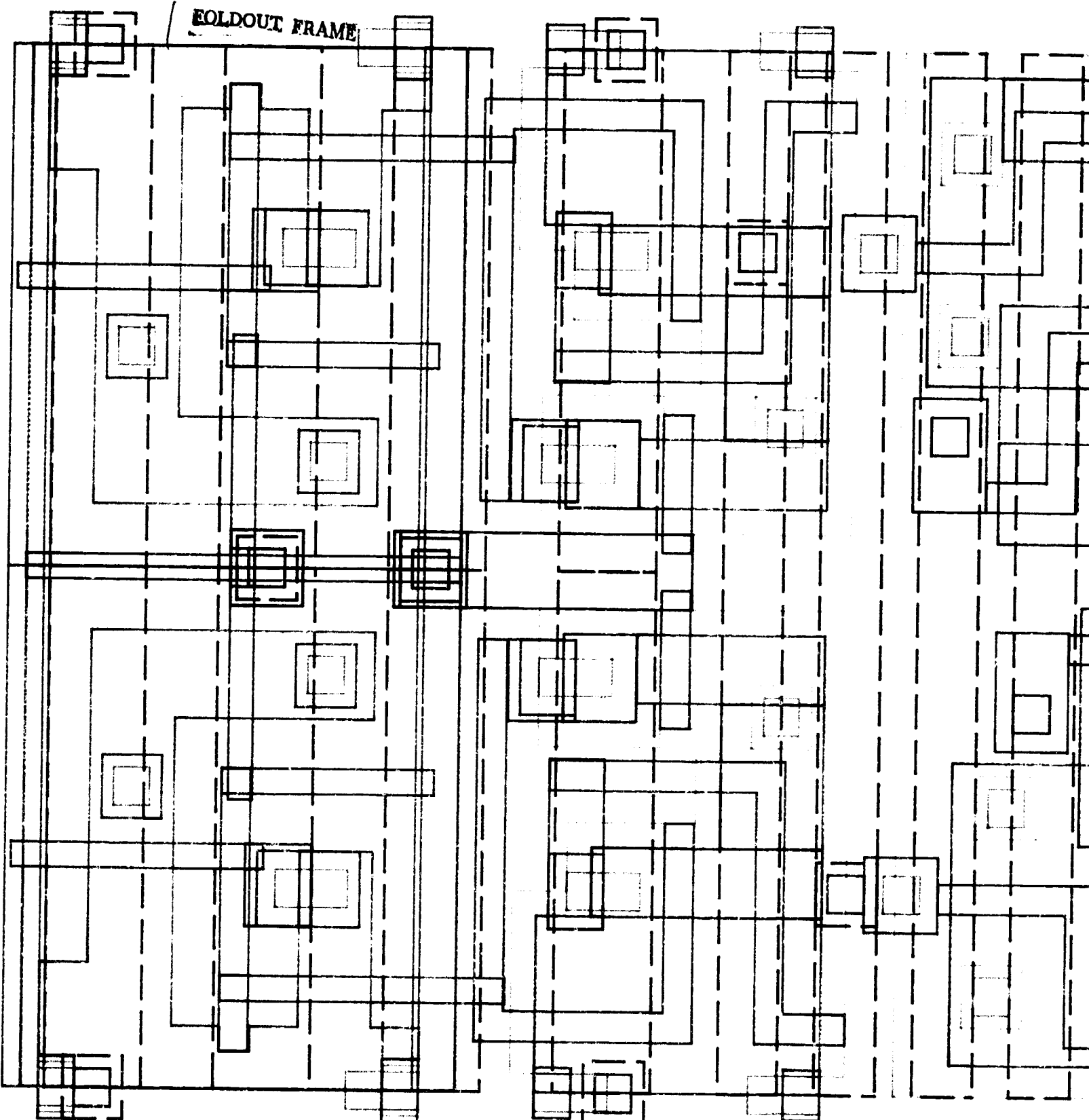
ODD CELL

10C4

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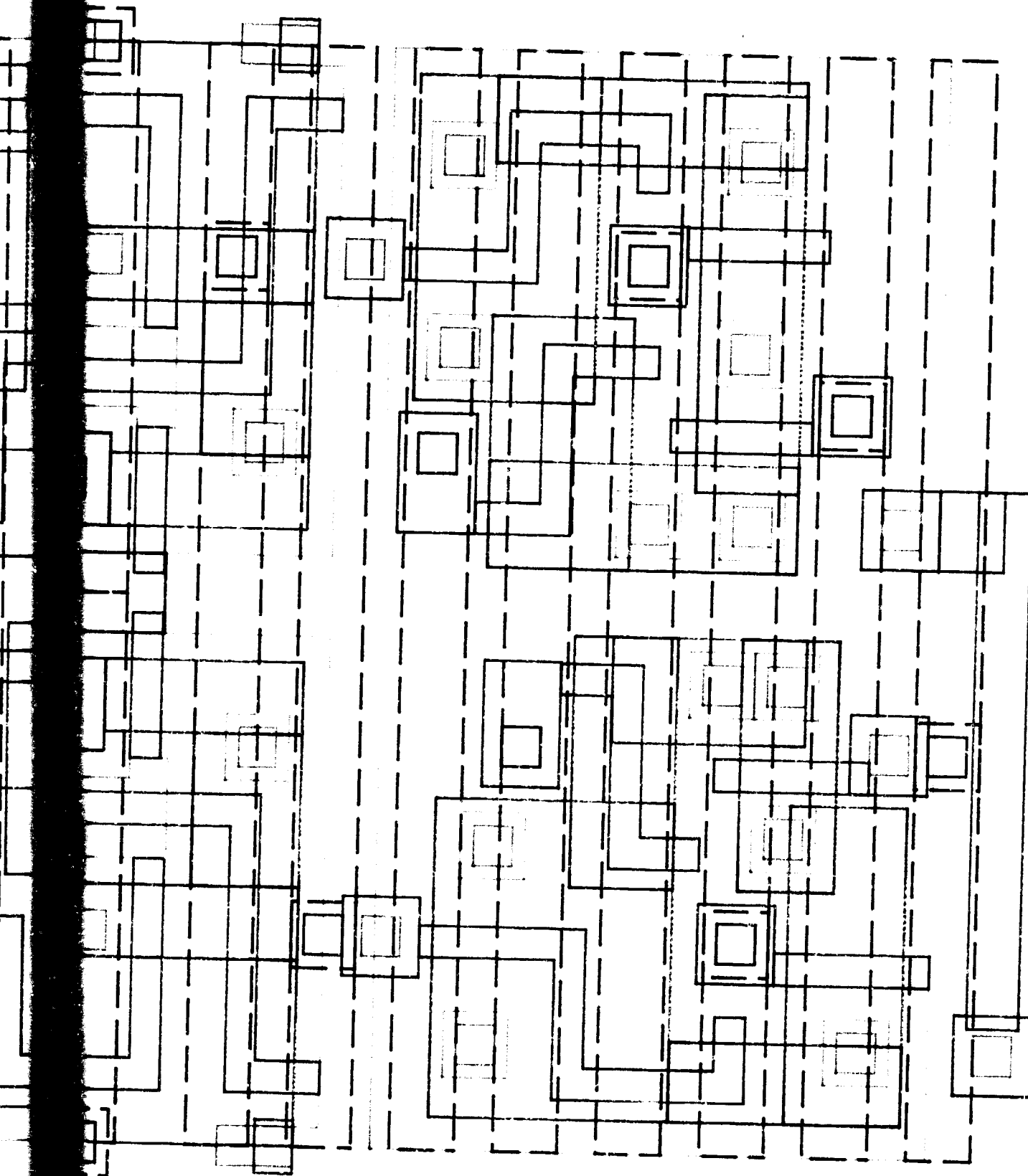
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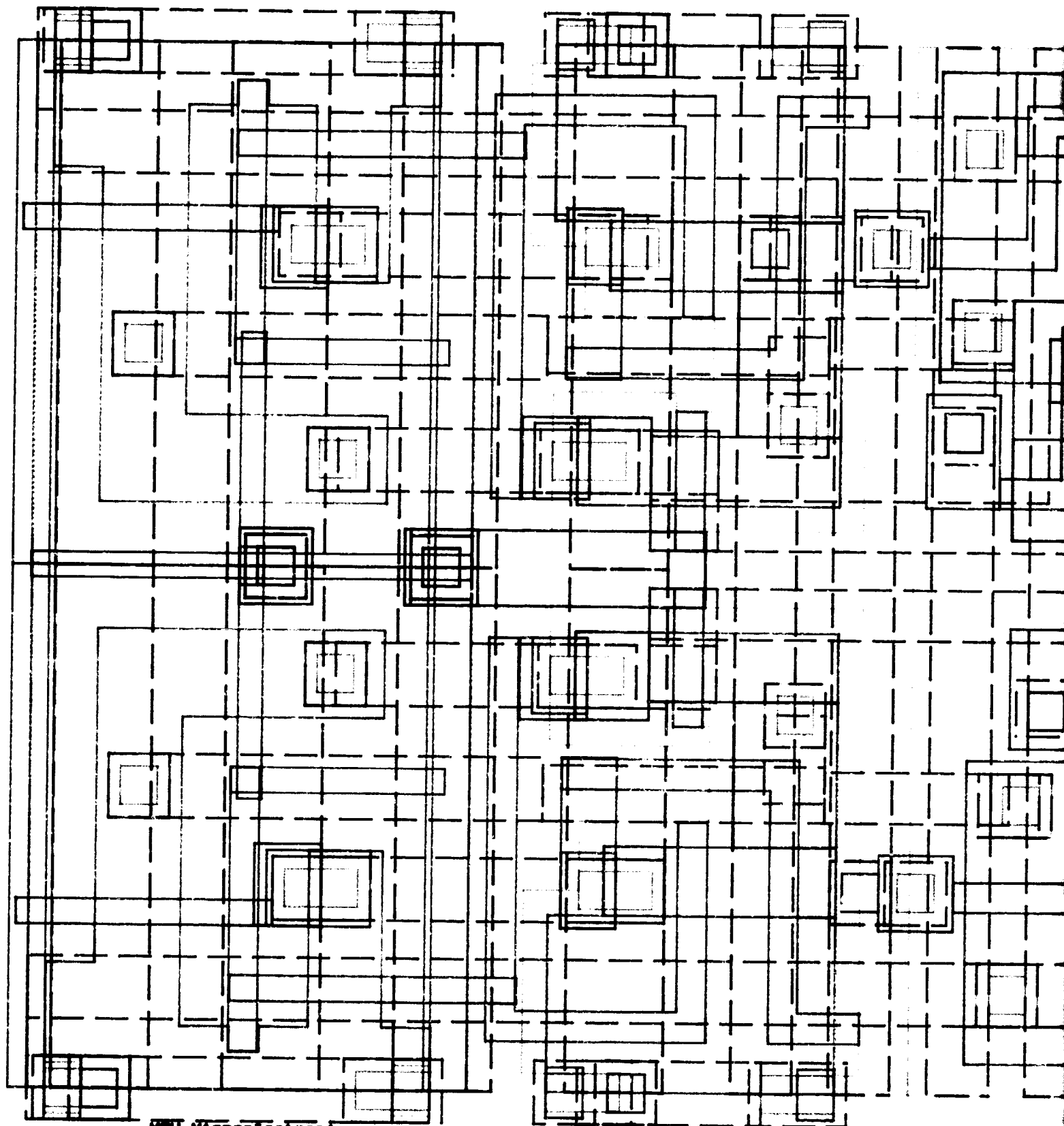


EVEN CELL

1005

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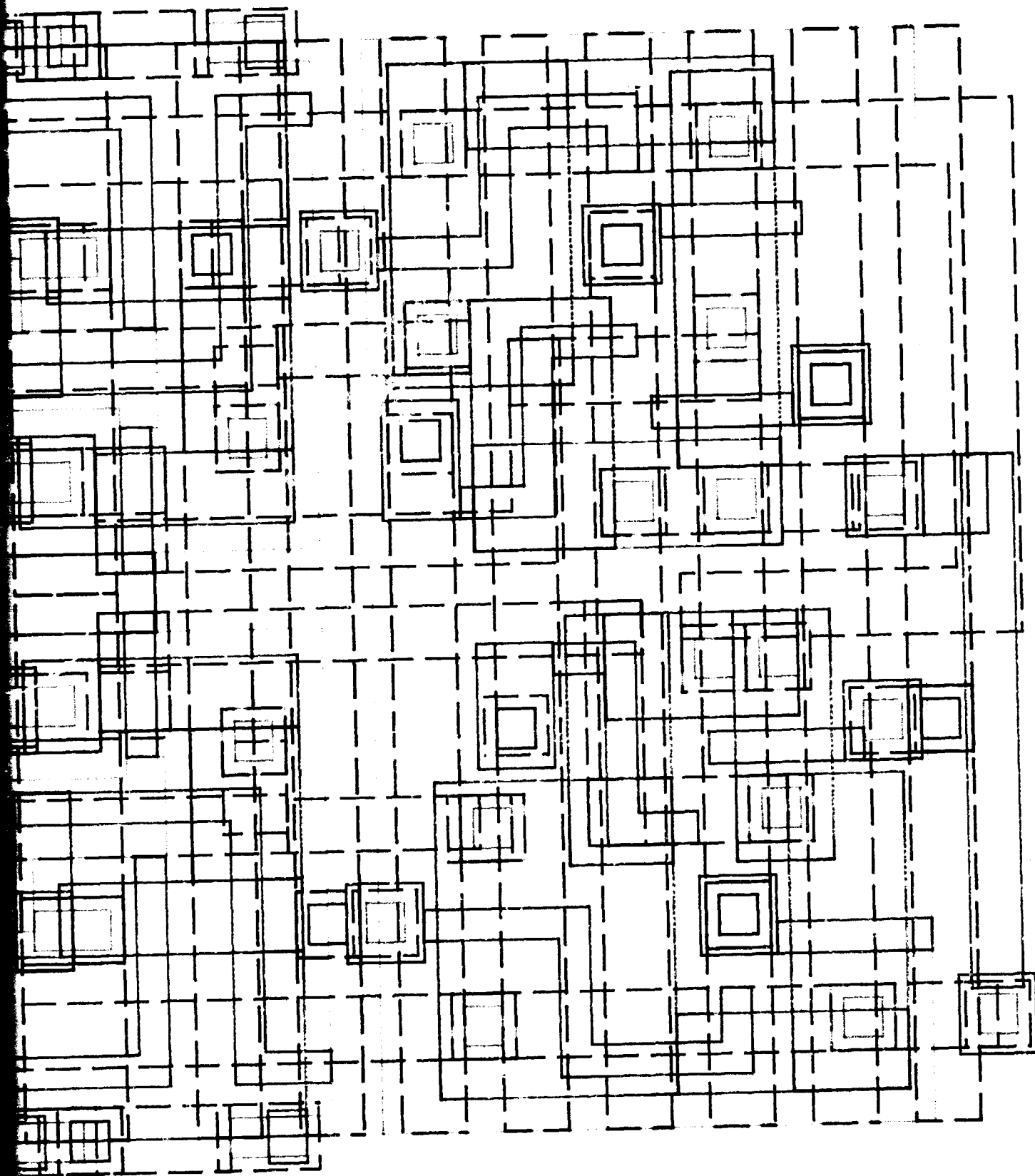
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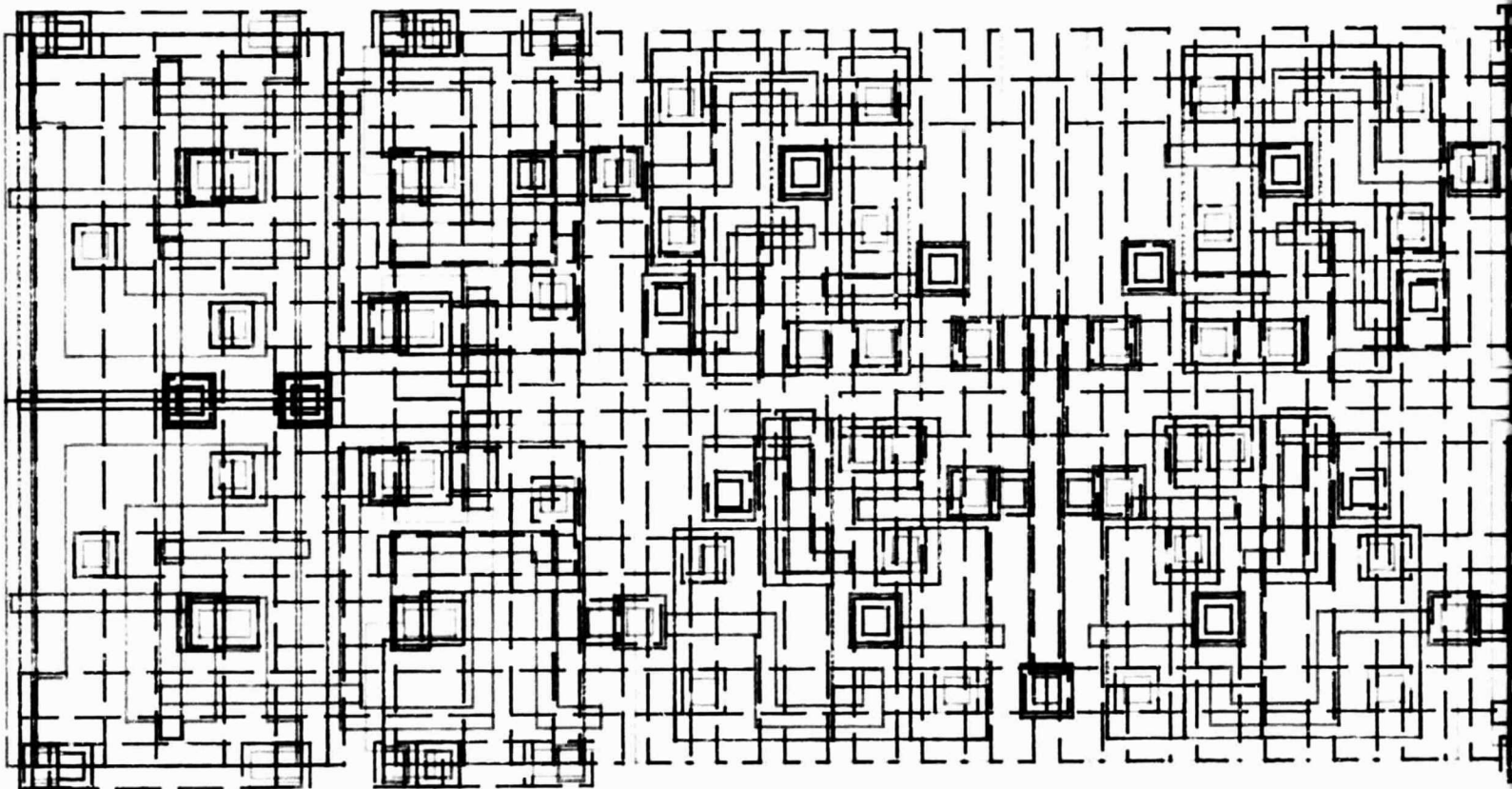
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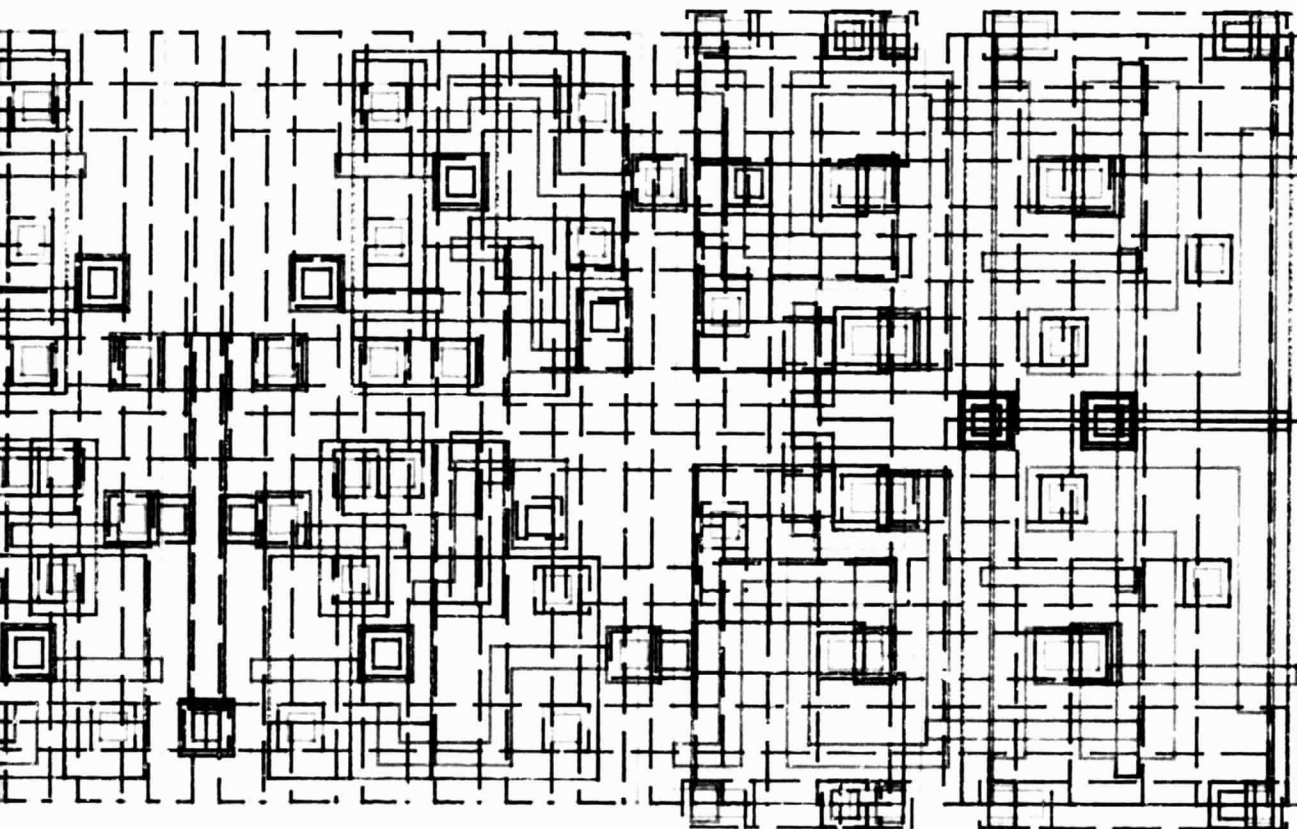
DUAL CELL  
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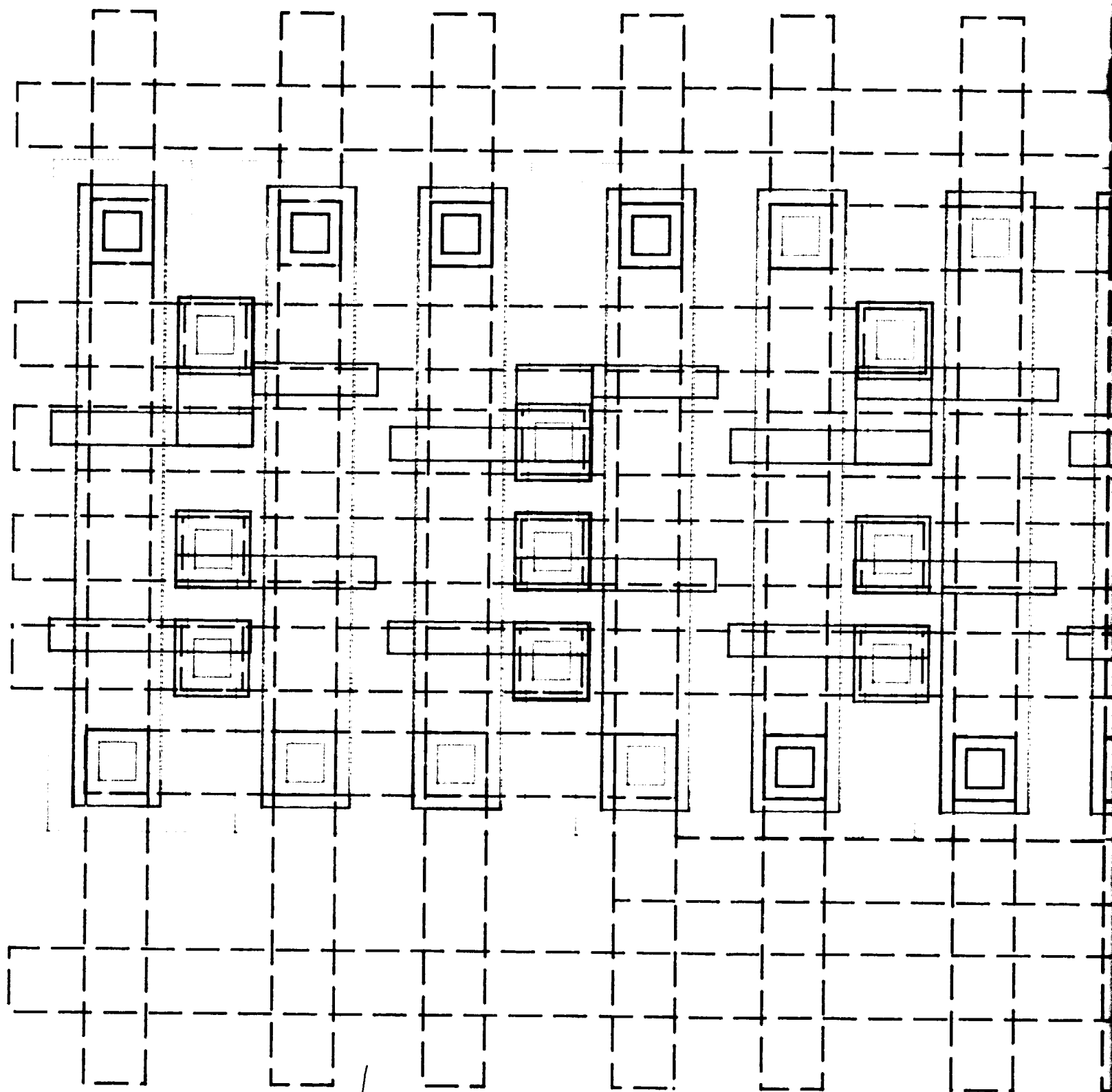


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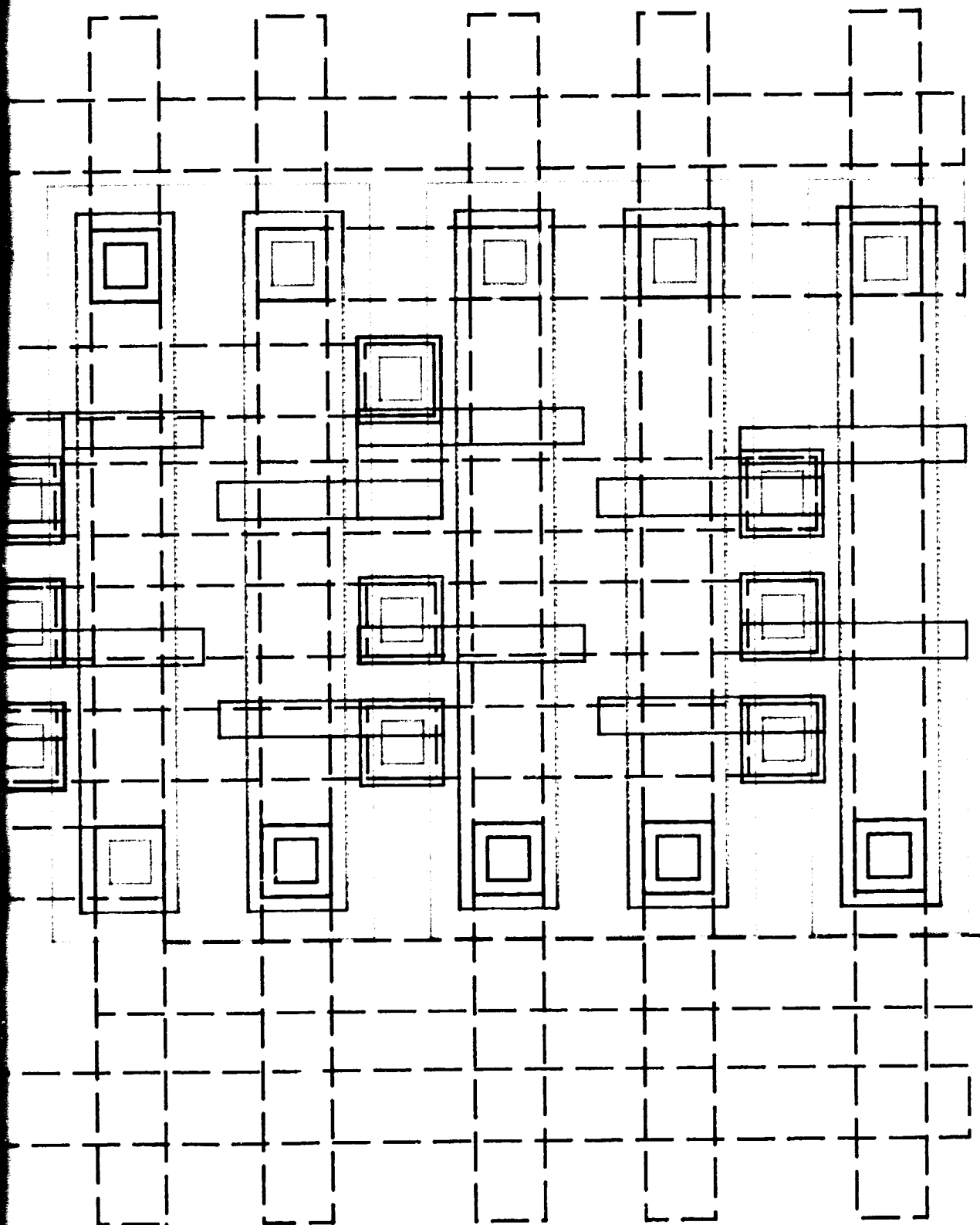
FUNCTIONAL BLOCKS P & K  
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P & K

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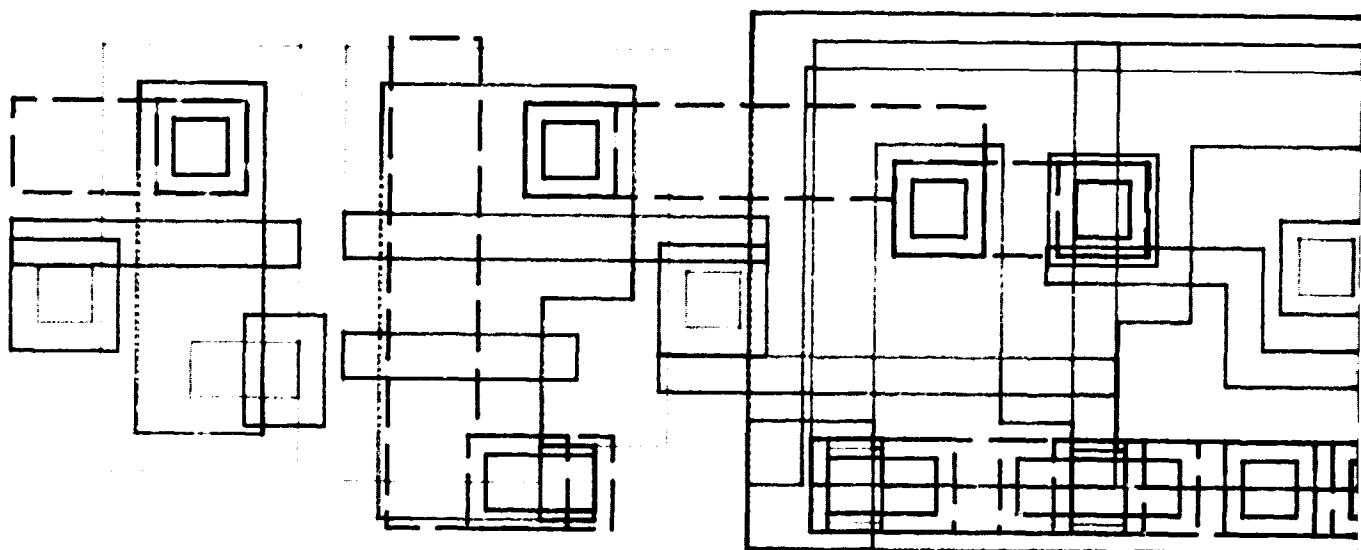
CONTROL BUFFER [ from Y=0 to Y=85 ]

10081

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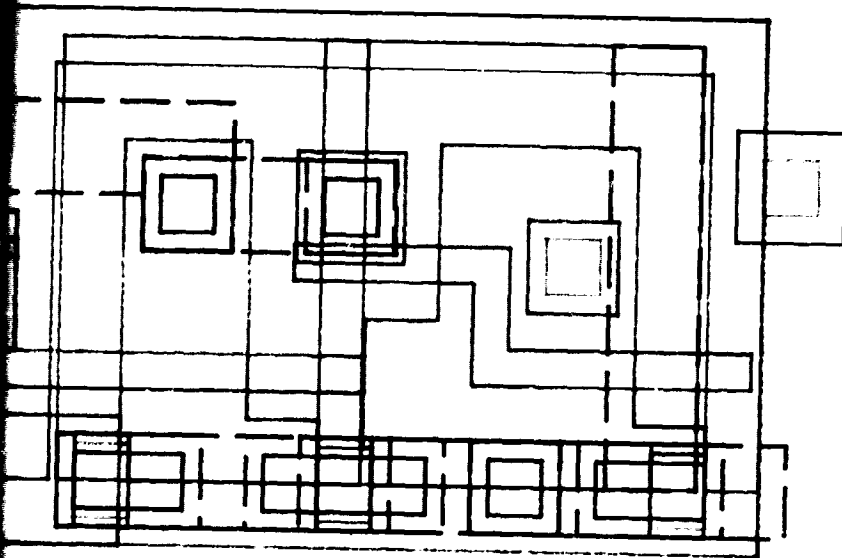
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Y=85 ]

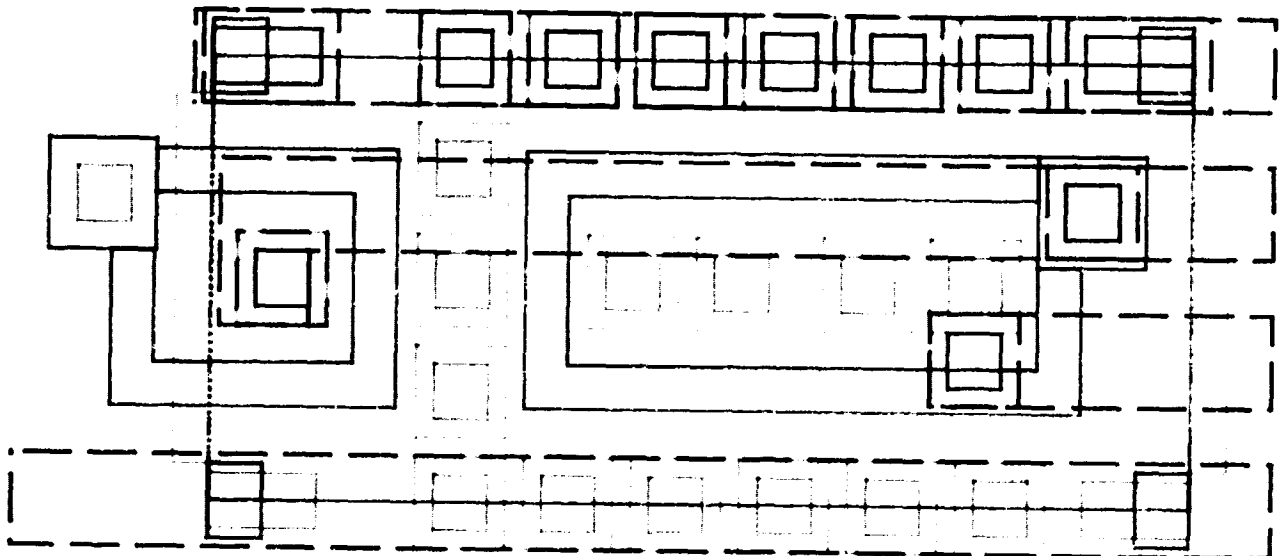
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CONTROL BUFFER [ from Y=85 to Y=150 ]  
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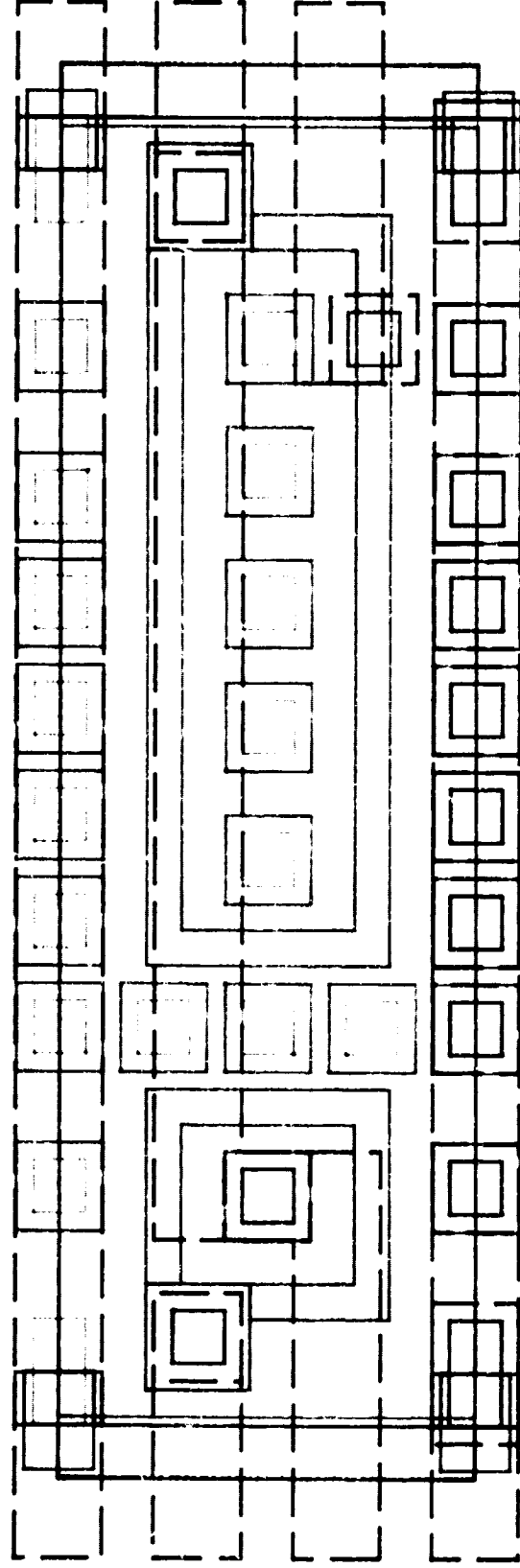


CONTROL BUFFER [ from Y=150 to Y=235 ]

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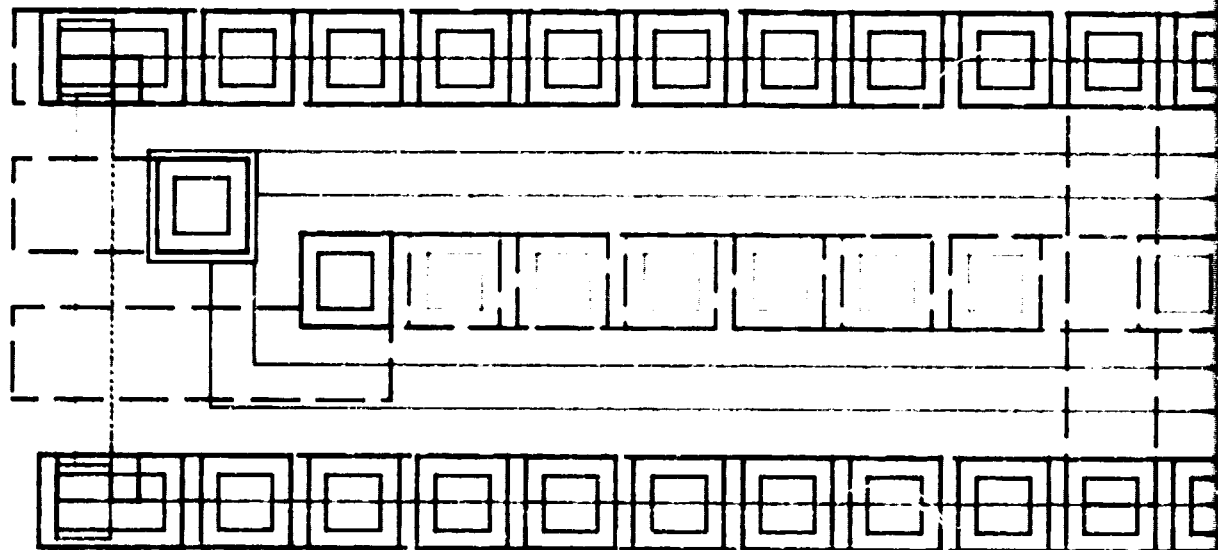
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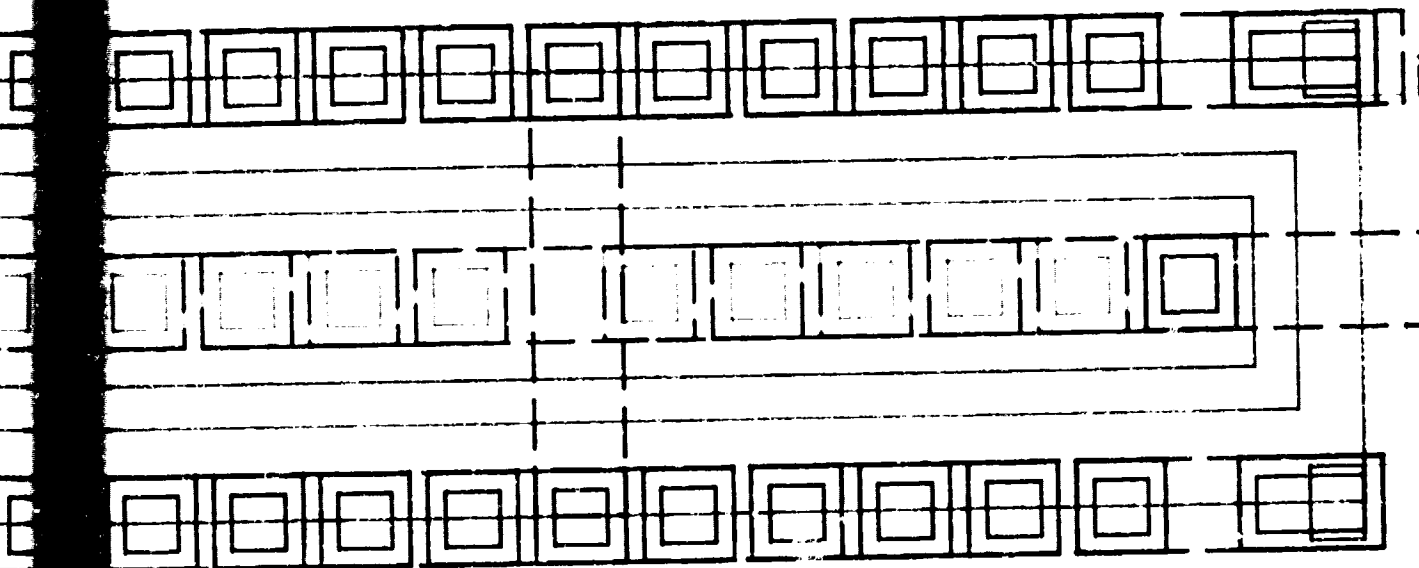
CONTROL BUFFER [ Y=235 to Y=340 ]  
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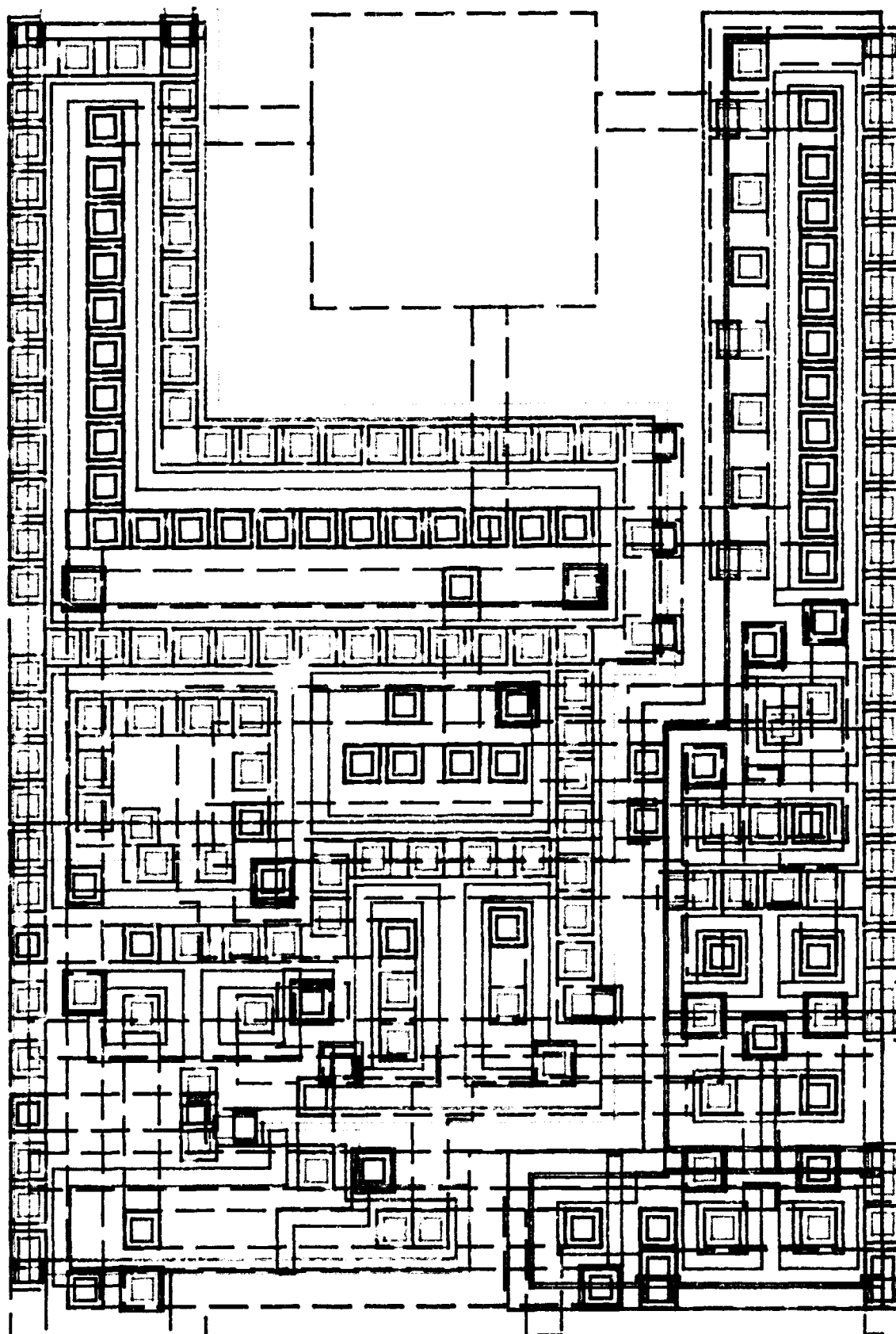


# I/O TRI-STATE BUFFER [ ENABLE CIRCUIT ]

1009

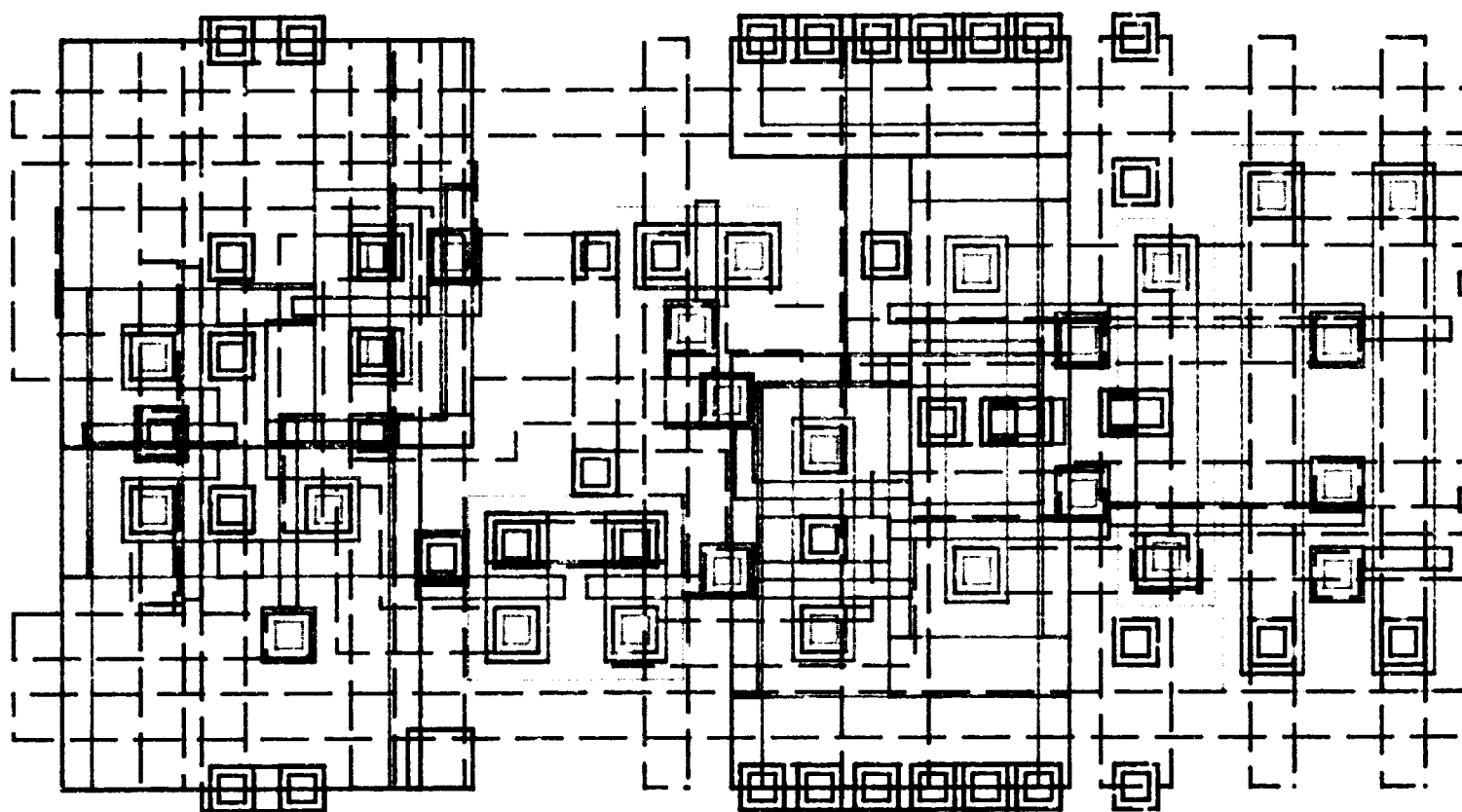
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CARRY CHAIN & R BLOCK [ path #1 ]  
10101  
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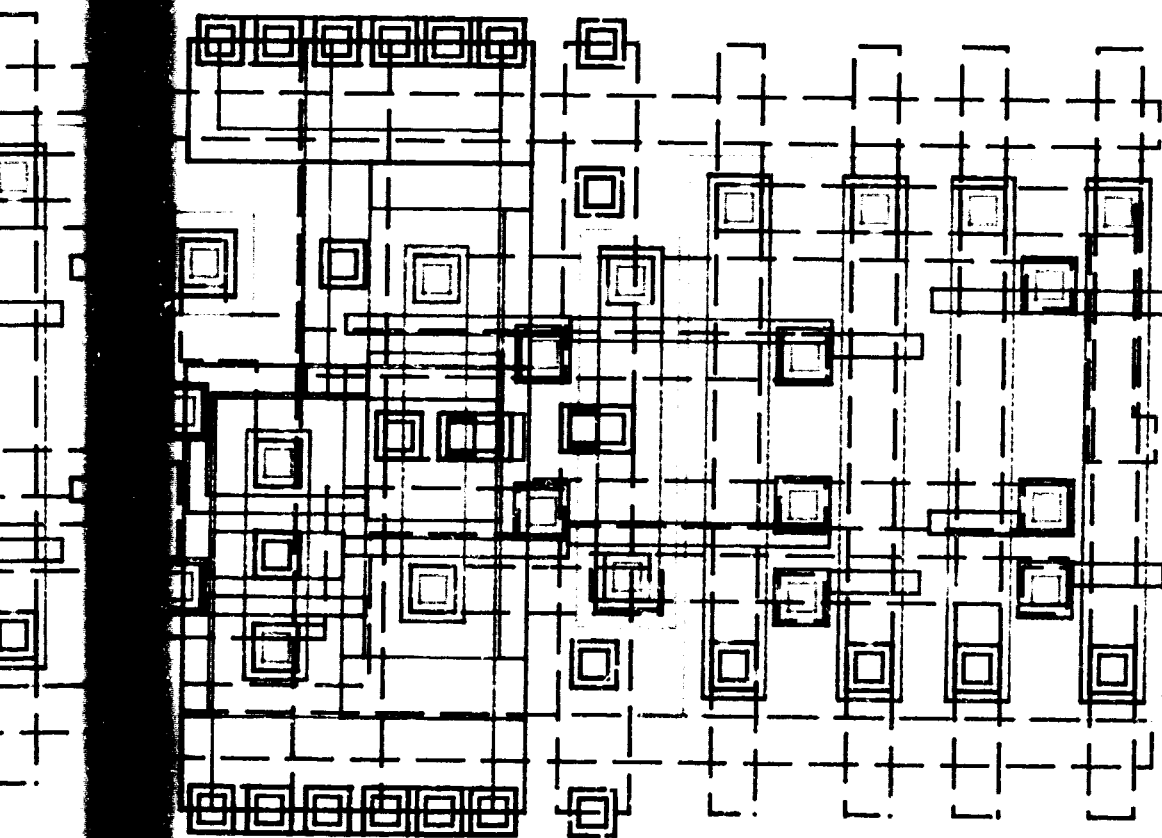


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path #1 ]

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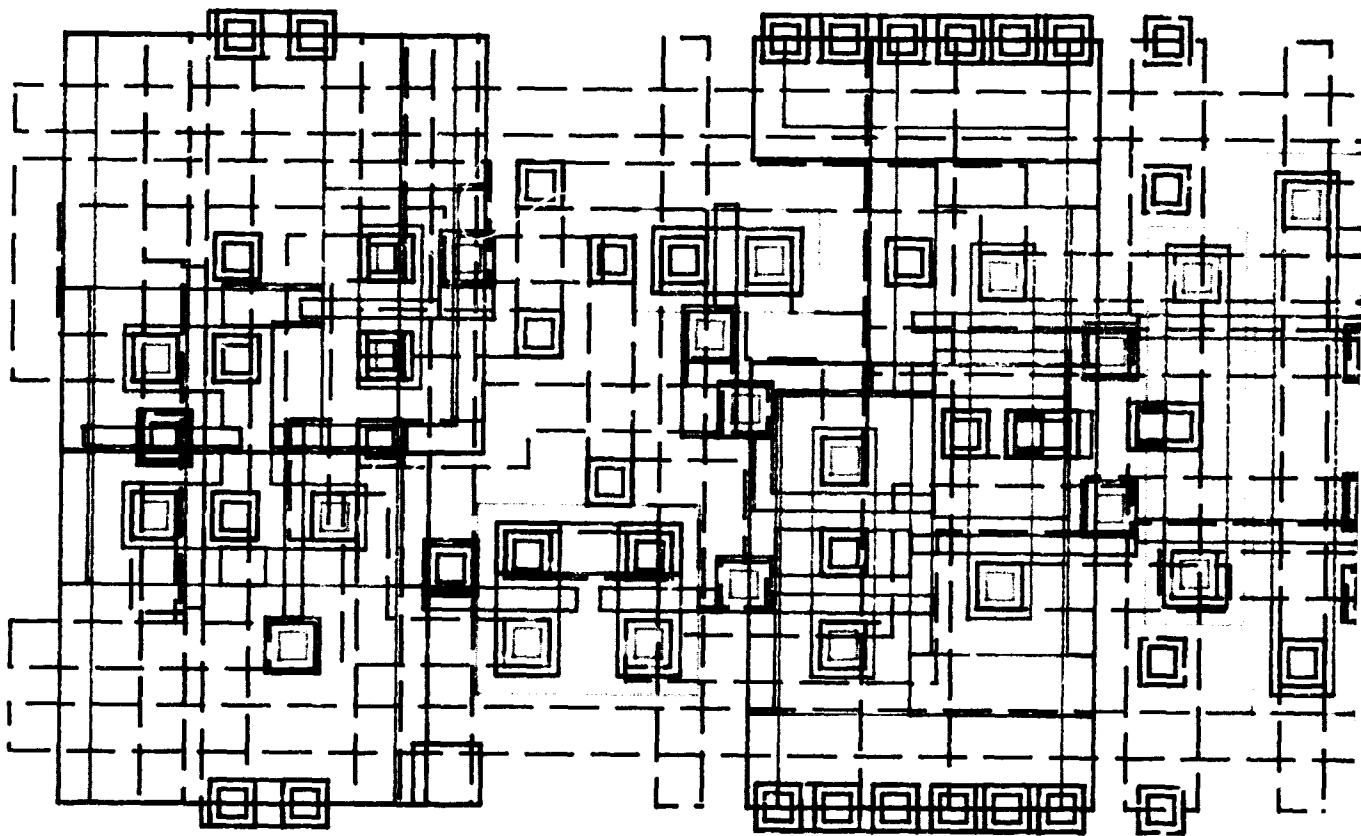
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CARRY CHAIN & R BLOCK [ path #2 ]  
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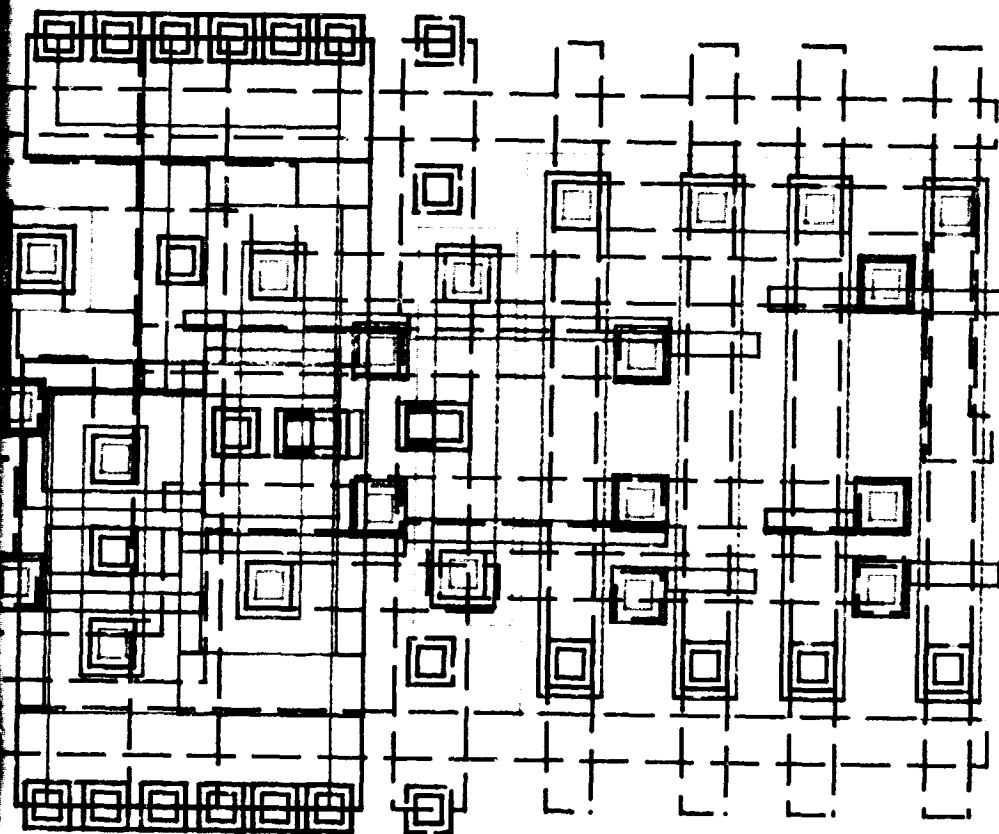
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path #2 ]

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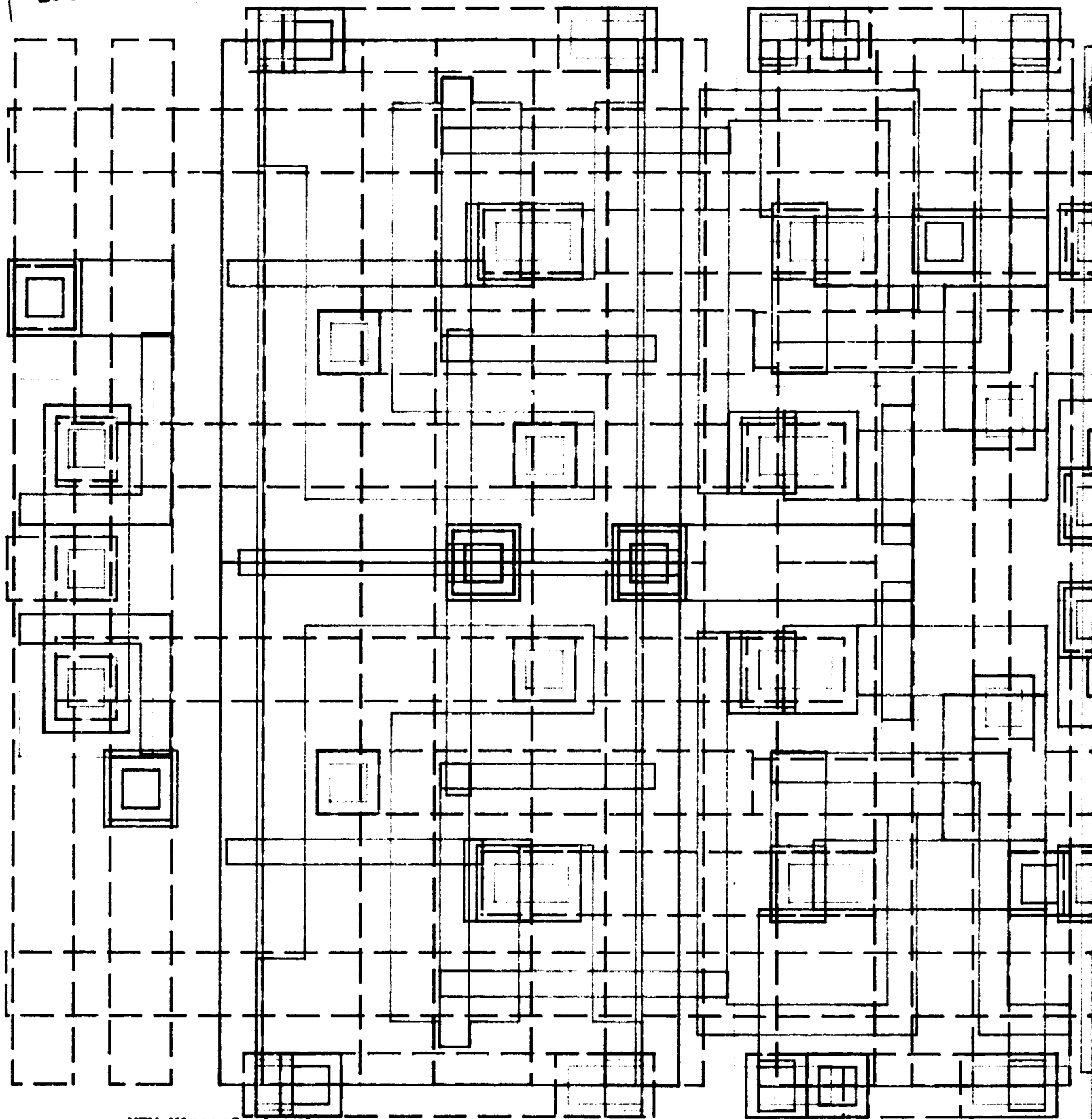
# OUTPUT LATCH to ARITHMETIC LOGIC UNIT

1011

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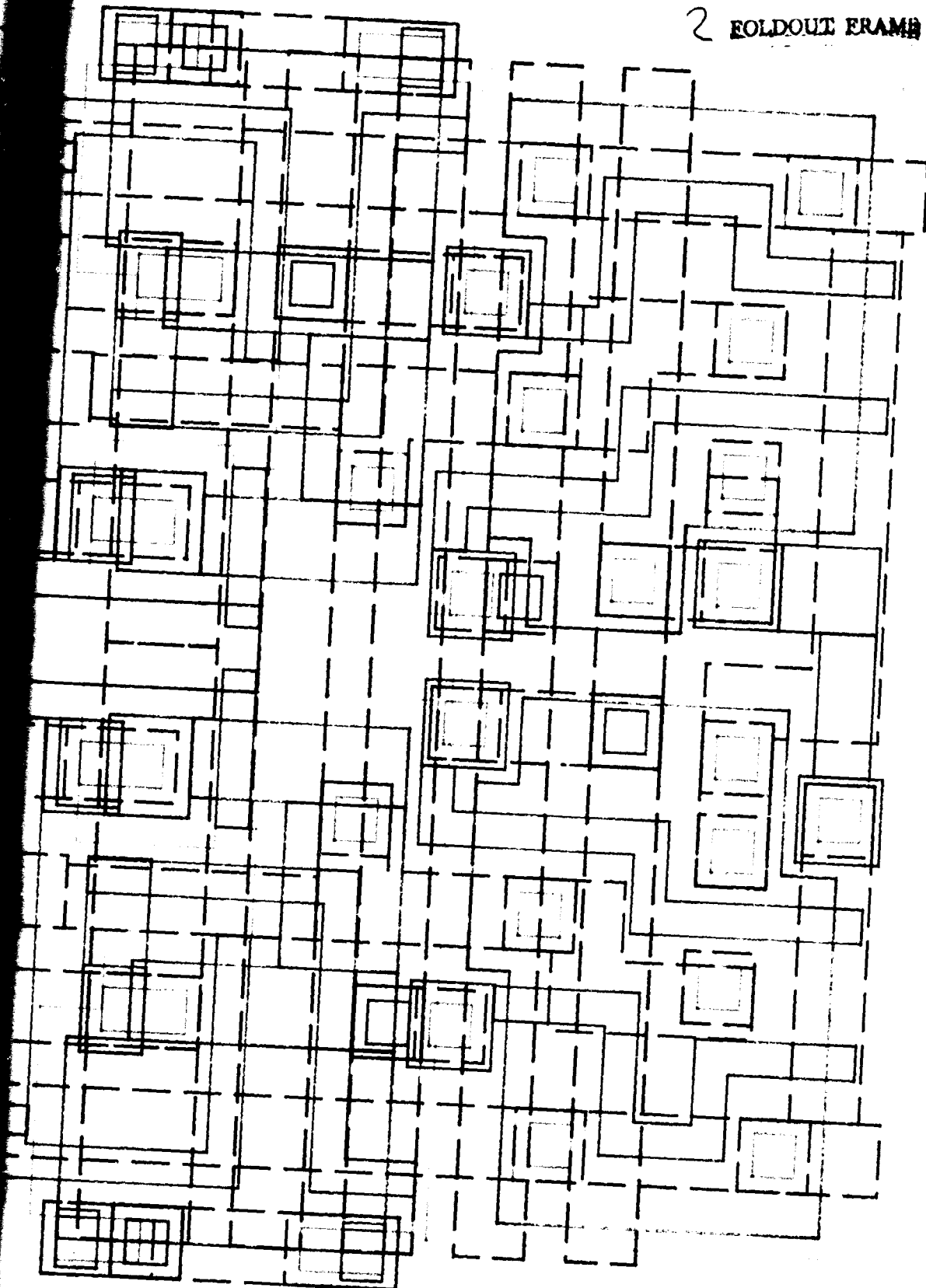


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# LOGIC UNIT

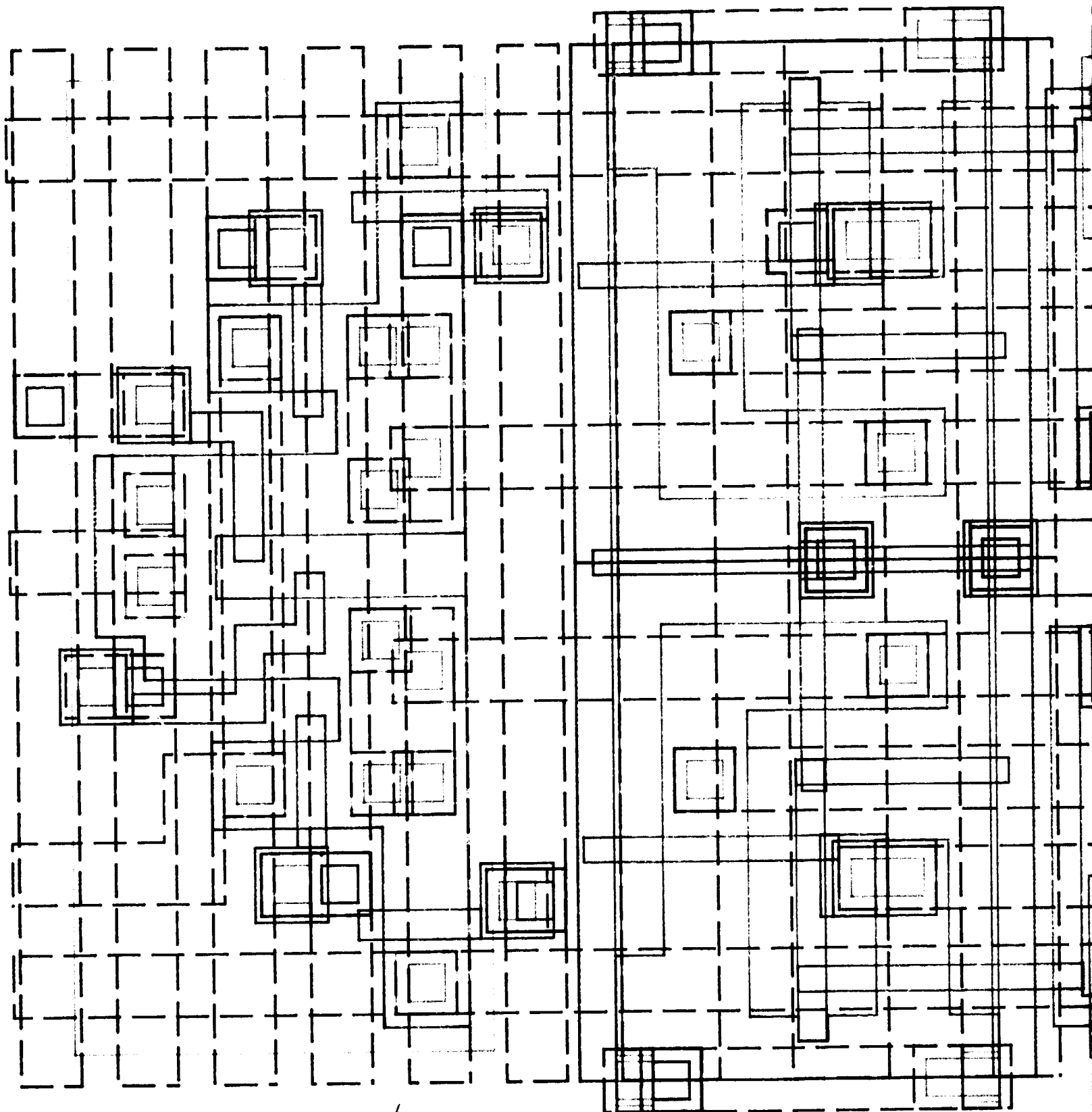
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INPUT LATCH to ARITHMETIC LOGIC UNIT  
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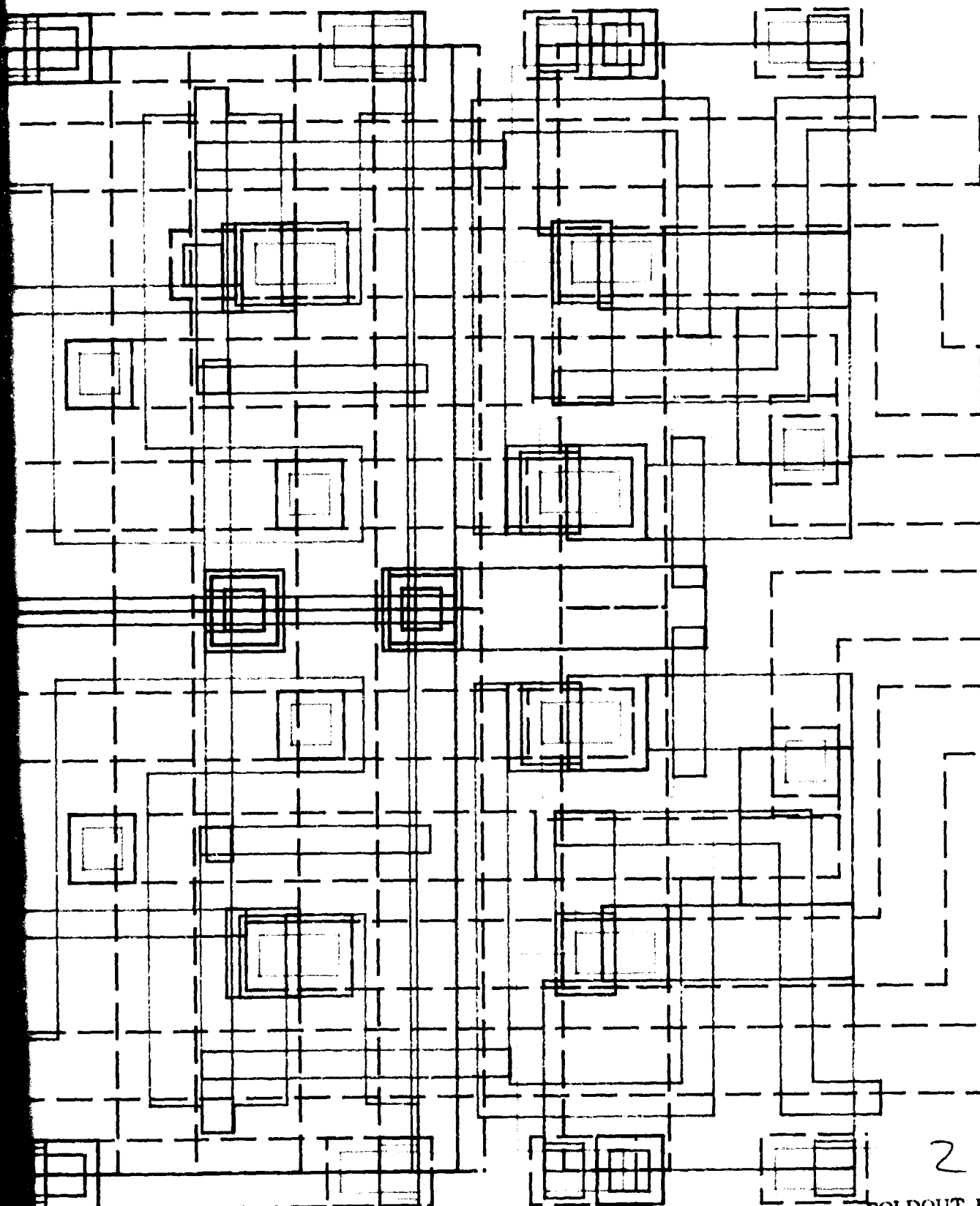
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# ETIC LOGIC UNIT

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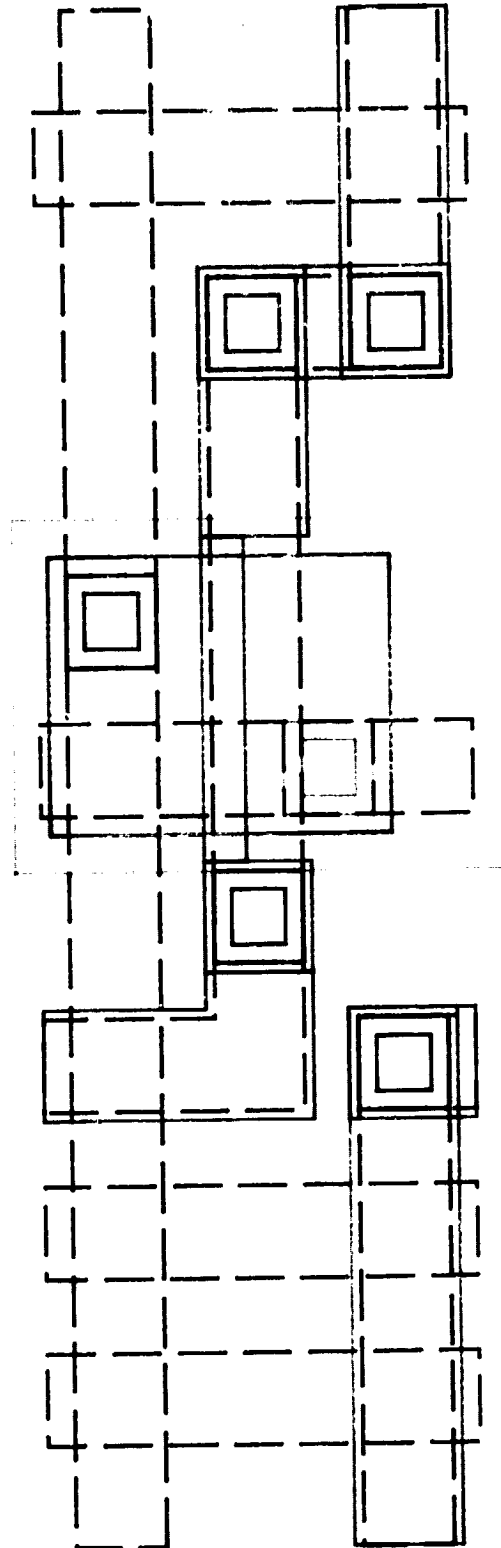


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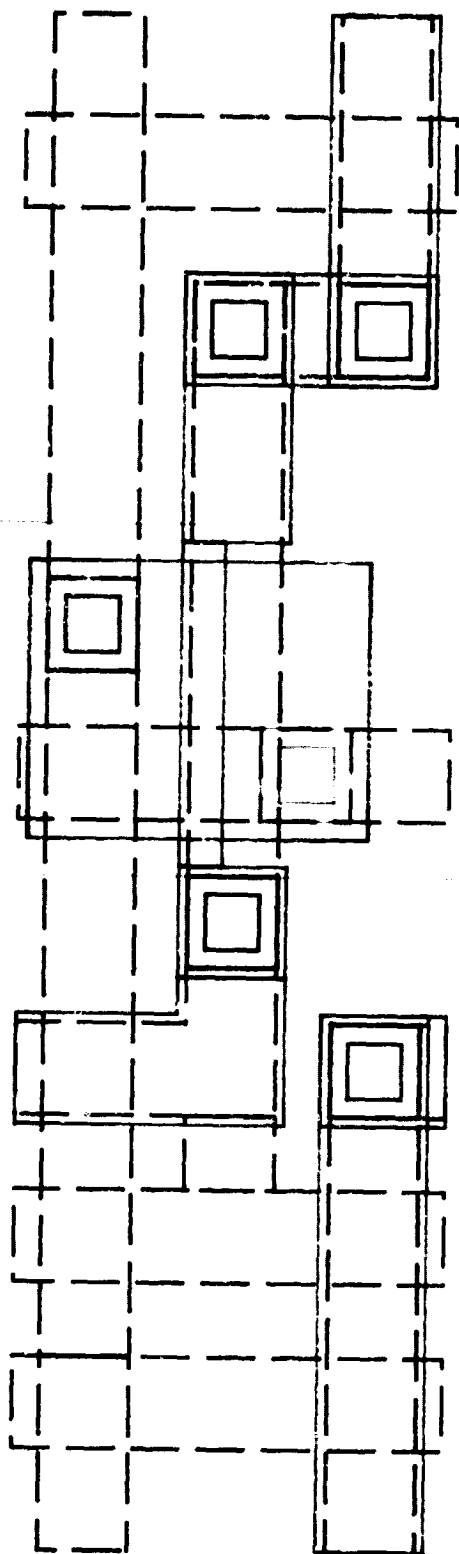
BASIC CELL for the SHIFTER  
1013  
scale: 1001X

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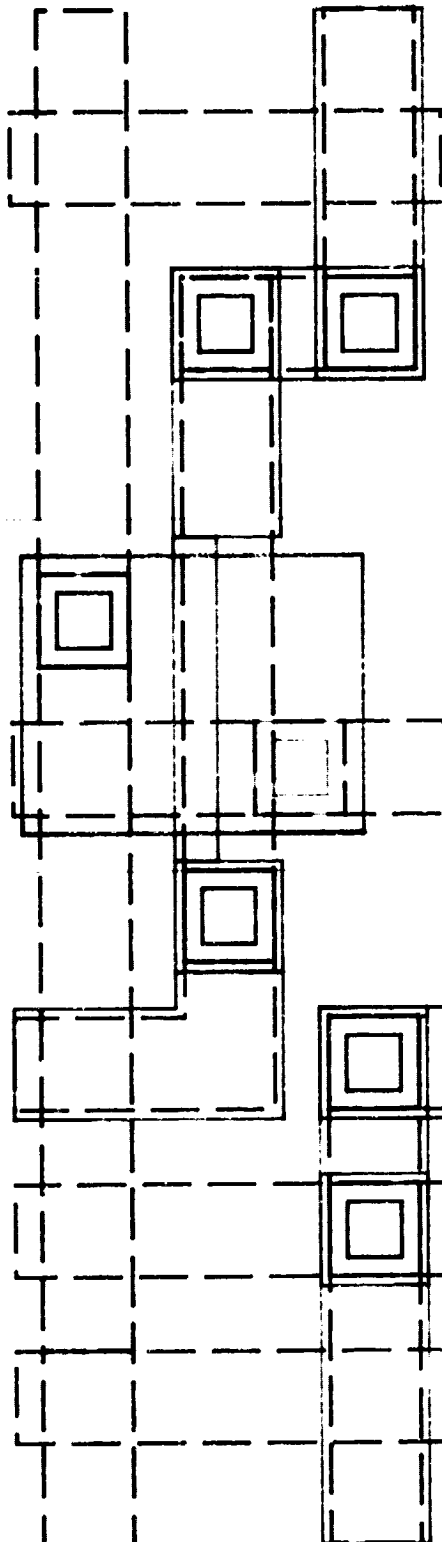
CELLS on the LEFT EDGE of SHIFTER  
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scale: 1001X

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CELLS on the RIGHT EDGE of SHIFTER  
1015  
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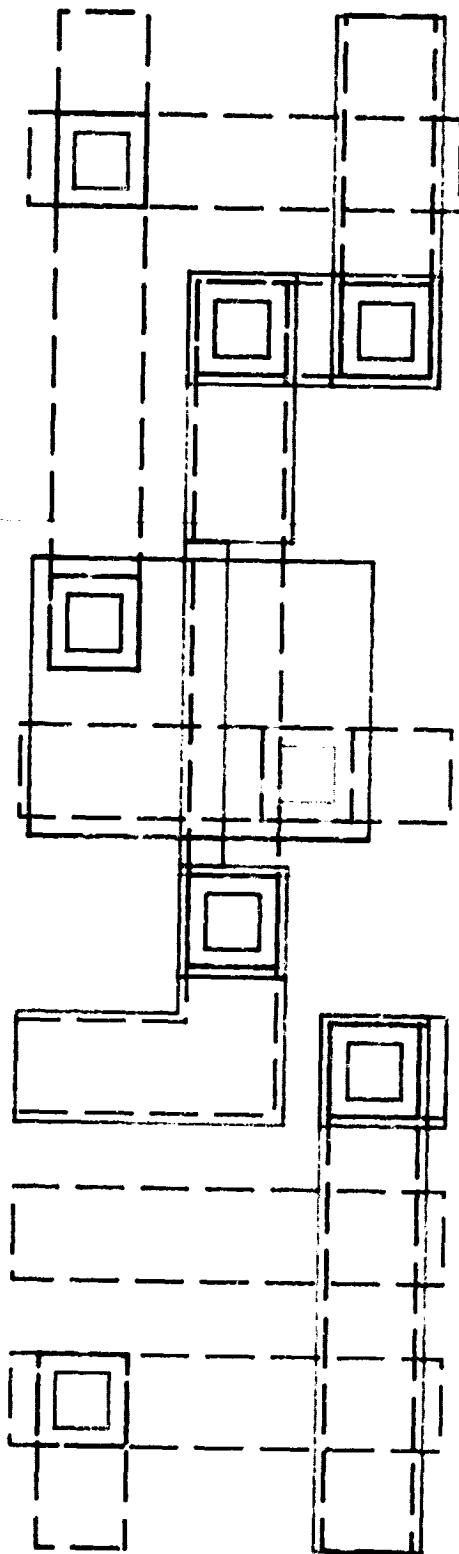
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CELLS on the DIAGONAL of SHIFTER  
1016

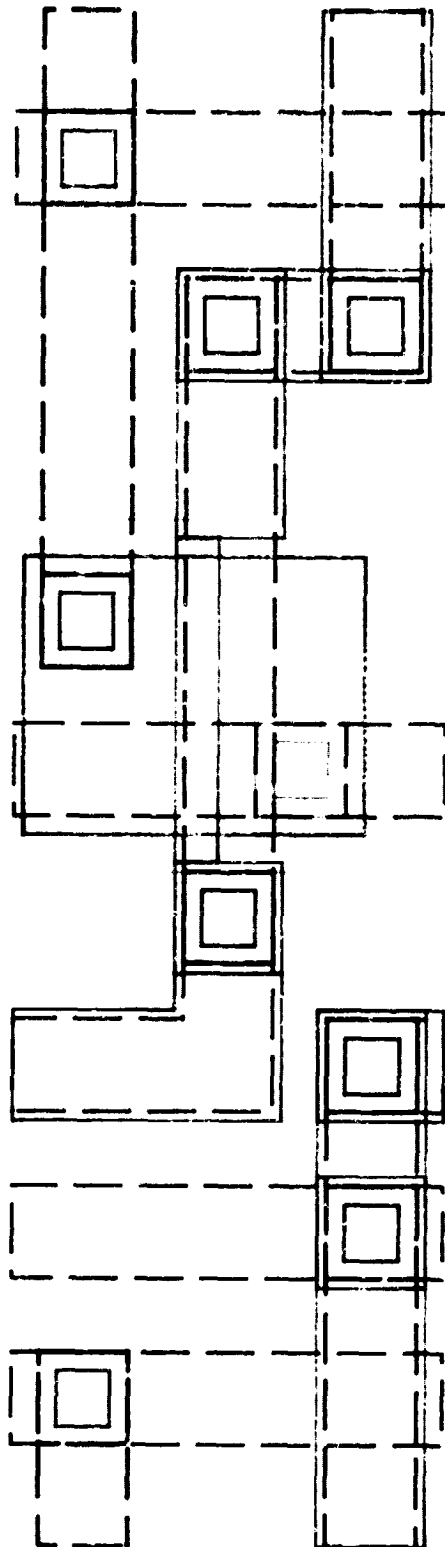
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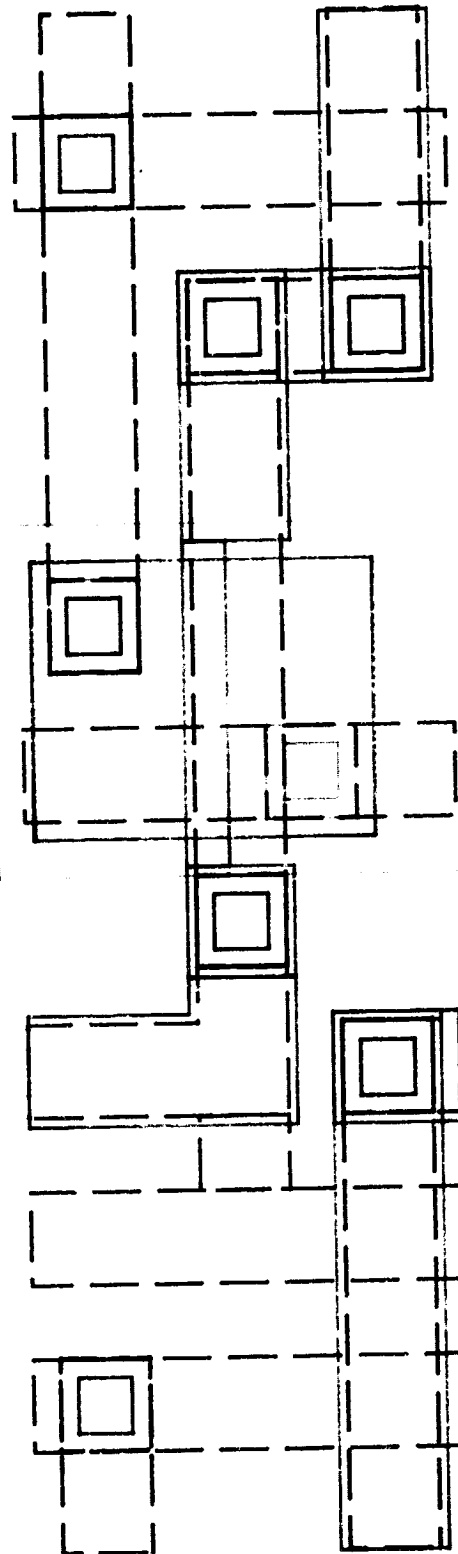
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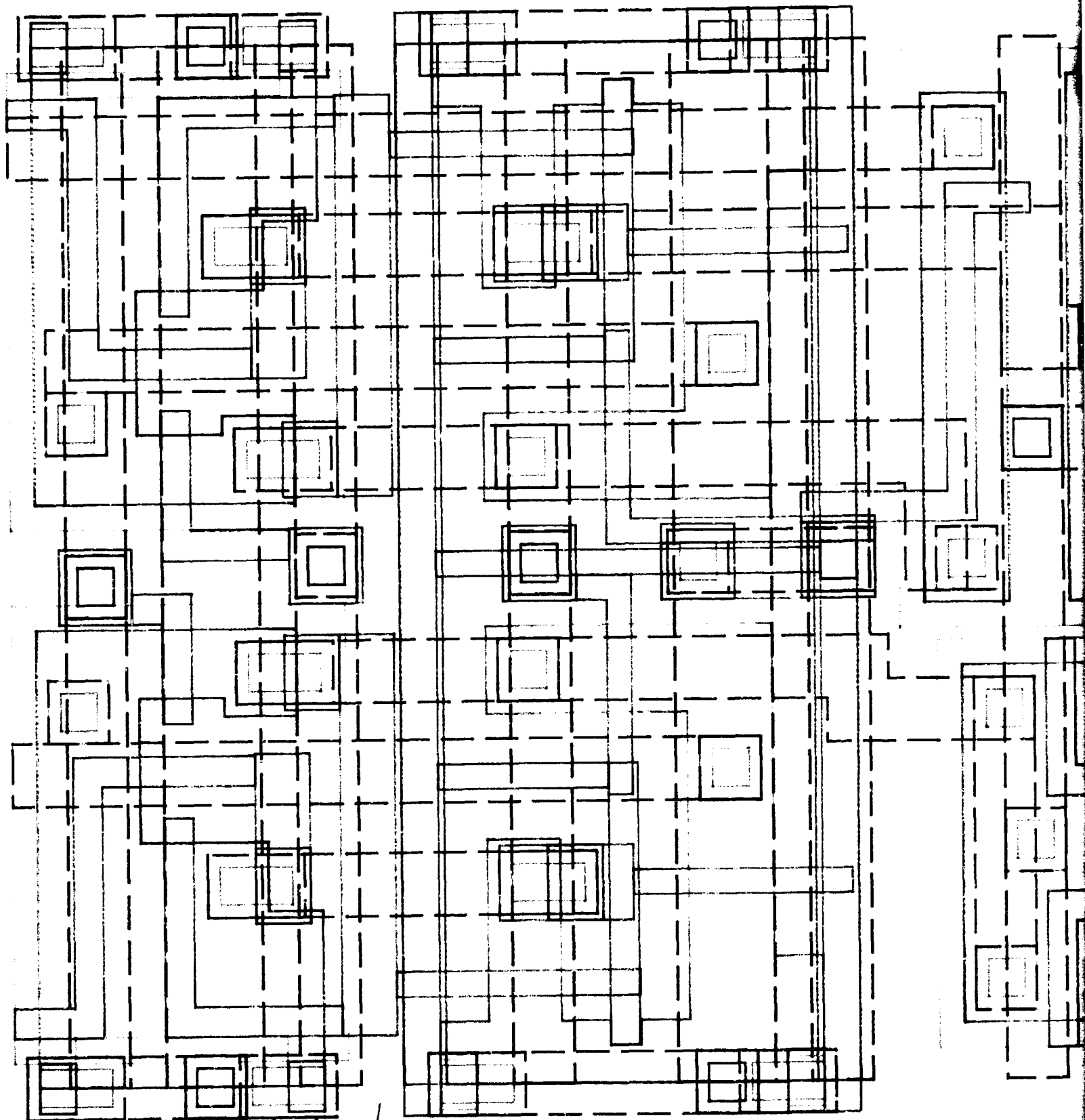
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I/O LATCH to TRI-STATE BUFFER  
1018  
scale: 1001X

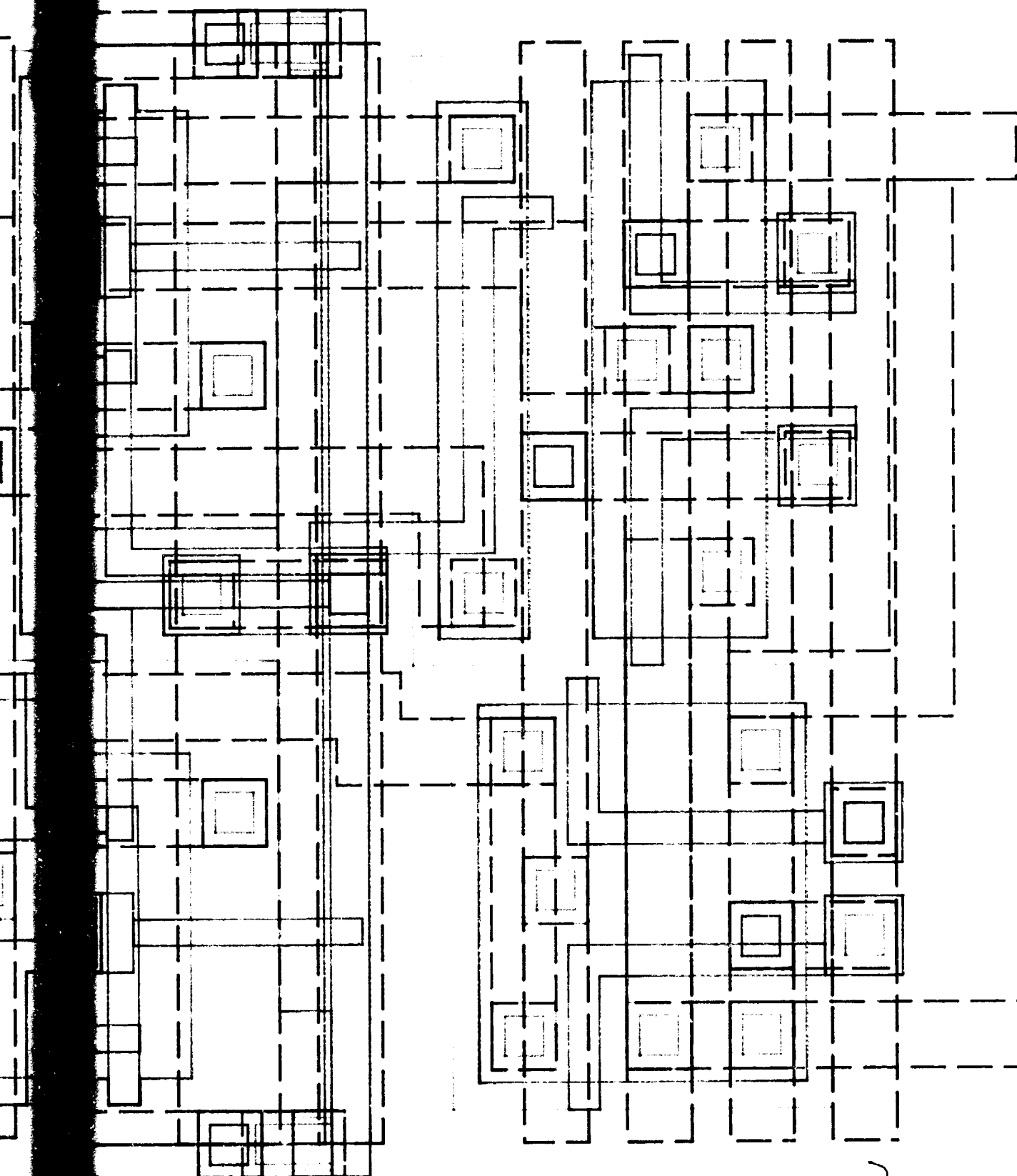
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BUFFER

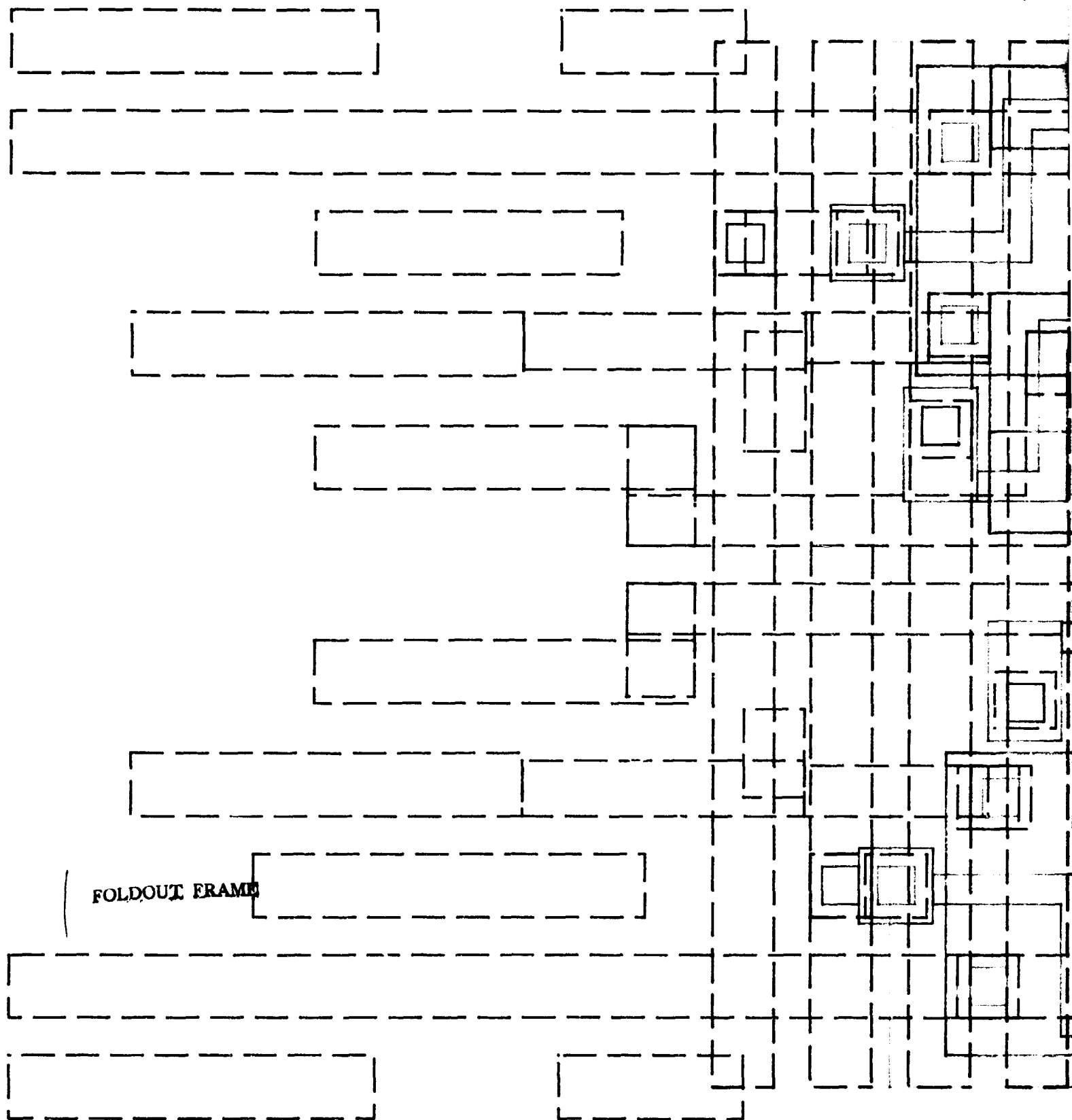
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MULTIPLEXER (adds silicide to latch)  
2002  
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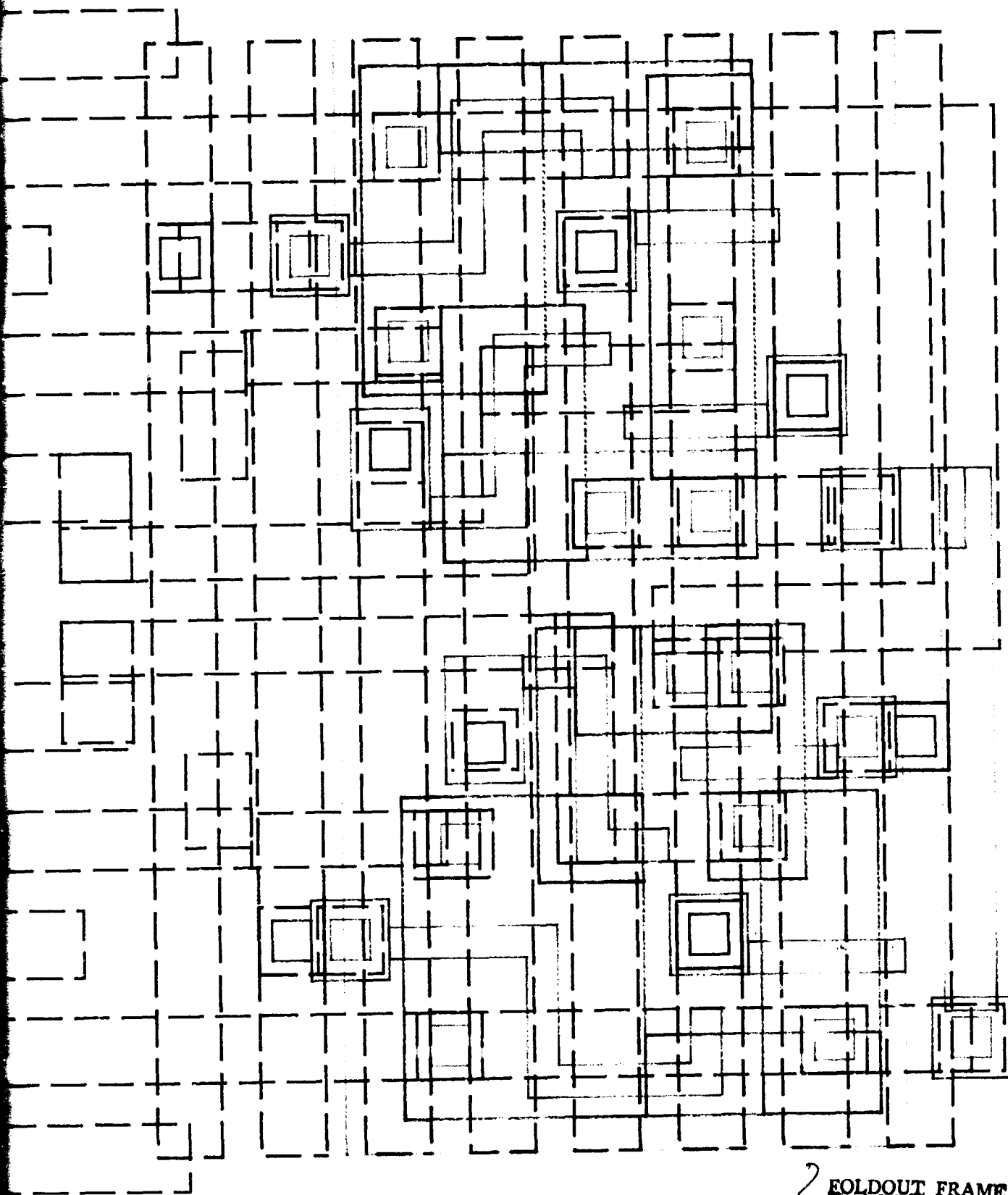
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alicide to latch)

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2 FOLDOUT FRAME

ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

Part 4: Stored Logic Arrays - SLAs Implemented  
with Clocked CMOS

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STORED LOGIC ARRAYS - SLAs  
IMPLEMENTED WITH  
CLOCKED CMOS

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STORED LOGIC ARRAYS - SLAs  
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SUMMARY

Stored logic arrays are folded PLAs with the AND and OR planes merged into one physical space. The structure is shown to be compatible with the STAR layout of transistors. As a result the STAR foundation wafers, or similar structure, can be used to implement the structured logic associated with PLAs. This structure offers the potential for implementing the control structure for the Mosiac Transistor Array. In addition the structure offers an organized approach for the distribution of logic gates in state machines and as such may represent an approach to untangling the placement and routing difficulties in random logic.

In order to efficiently compact the logic onto the regular grid of the STAR, it is necessary to develop a new style of CMOS circuitry which does not utilize the classic CMOS pair of transistors for each fan-in. A clocked variety of CMOS is developed which achieves higher layout density and performance. Concepts of simultaneously precharging a series of gates are developed. At an appropriate clocking signal the logic is evaluated with the signals "rippling" through the logic. This concept has led the author to the term "ripple" logic. It is shown that the logic is not general; consequently, the compromises are developed relative to high performance, regular logic arrays. Since dynamic techniques are utilized, careful considerations of charge splitting are observed. As such, clocked CMOS concepts are presented in a form suitable for the uninitiated readers.

STORED LOGIC ARRAYS - SLAs  
IMPLEMENTED WITH  
CLOCKED CMOS

I. Introduction

Gate arrays have become increasingly popular in the last few years as a means of implementing complex logic with reduced engineering cost. The NASA STAR is a double-layer metal CMOS version of a gate array. The STAR has at least two features which offer consideration of an alternate design approach: 1) The STAR is composed of rows of NMOS transistors and rows of PMOS transistors with the neighboring transistors always coupled via the source/drain diffusion. 2) The gates of the transistors are left unconnected through the standard layers and are connected with the programming mask levels. Array logic such as programmable logic arrays (PLAs) or storage logic arrays (SLAs) offer an organized means of placement and routing for logic with some sacrifice in performance.

Classic CMOS circuitry requires signals to drive pairs of transistors instead of one, as normally used in NMOS. This requires greater area for interconnections and transistors. However, clocked CMOS, with the concept of precharging circuit nodes and then conditionally discharging them, requires only one transistor per signal input. Furthermore, it offers the potential for speed enhancement. A requirement for this circuit style is that the gates for NMOS and PMOS pair transistors remain uncommitted, a feature found in the STAR design.

An SLA is a particular variety of PLA which is folded with the OR and AND planes merged together. The latches ( or flip-flops ) can be placed around the logic array. The actual size of the AND and OR gates for particular signals can vary with the actual applications, thus providing folding opportunities not normally found in PLAs. The STAR design offers the potential of implementing the SLA on its standard structure. The SLA design can be part of a STAR chip design and merged in with conventional gate implementations.

With these concepts in mind the SLA design is pursued.



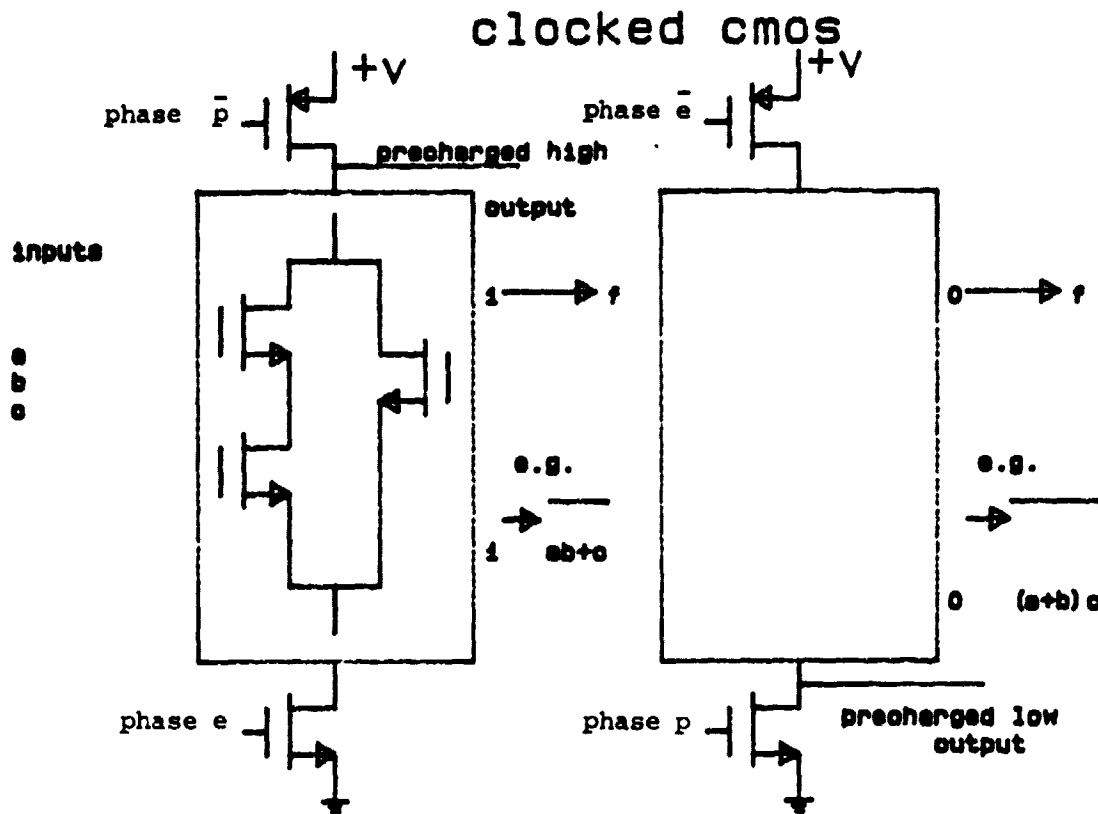
## II. Clocked CMOS

### A. Basic Concept

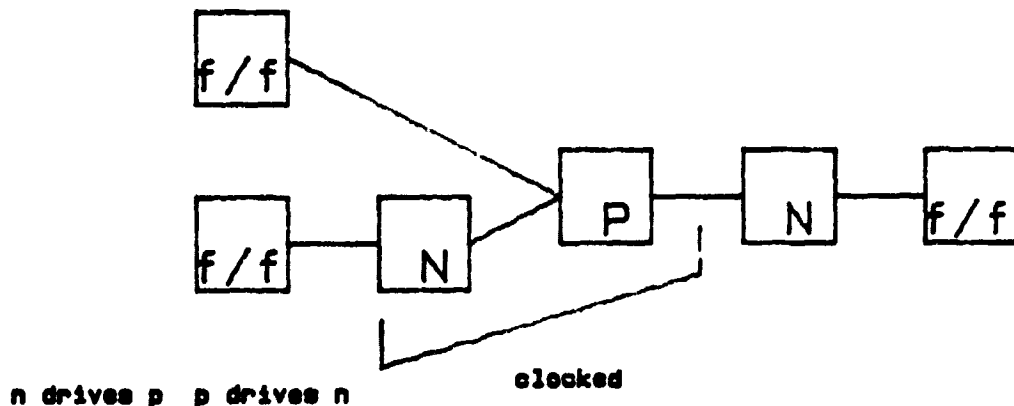
There are several clocked CMOS circuit styles. All are based on the concept of precharged gates. Defining an N-Gate as a clocked CMOS gate which utilizes NMOS transistors for logic evaluation, one simply uses a PMOS transistor to precharge the output unconditionally to the positive supply potential during some precharge clock signal and conditionally discharges the output back to ground through a series-connected NMOS transistor which is switched on with an evaluation clock signal. If the series/parallel combination of NMOS transistors which form the logic function offers a path to ground, the output is discharged during the evaluation period. If the logic devices do not offer a conduction path or the evaluation device is not turned on, the output remains in its precharged state subject to the leakage discharge of the node. This leakage time constant can be expected to exceed 1 msec with typical values being in the order of one second. This information associated with the charged state of the output is dynamic in nature and requires sampling with appropriate timing constraints. One can realize the logic function of the gate by noting the condition associated with discharge is producing a "0", for positive logic. If two devices are in series, both must be on for discharge, resulting in the NAND function being realized. If devices are in parallel, either can discharge the output; hence, the NOR function is realized. The more general parallel/series arrangement can be analyzed in a similar manner.

The P-Gate is defined in a dual manner to the N-Gate. The logic-forming transistors are implemented with PMOS devices and the precharging load device is a NMOS transistor. The output is unconditionally precharged to the "0" state and conditionally charged to the positive supply through the PMOS logic during the evaluation period. With series PMOS logic transistors the logic formed is the NOR function, assuming positive logic. With parallel logic transistors the logic formed is the NAND function. In general, the series-parallel combination of PMOS transistors must be the dual of the parallel-series combination of NMOS transistors for a given logic function, just as for classical CMOS.

Consider the following concepts illustrated in Figure 1: The information in the state flip-flops is stored in more-or-less conventional CMOS latches with active output drive in both directions. Local feedback in the latch provides indefinite retention of the information. The clocked P-Gates and N-Gates are precharged to their



n-gate definitioning p-gate  
concept



standby information is stored in static f/f's and clocked gates are precharged  
evaluation takes place in one clock period in a ripple through manner

FIGURE-1 CLOCKED CMOS CONCEPT

appropriate levels during the precharge or stand-by period, a period which can last an indefinite time since the state information is stored in static latches. N-Gates drive P-Gates and vice-versa. Similar gates never drive each other, e.g., N-Gates never drive N-Gates. One observes that the clocked gate inputs, if driven from an opposite type, are precharged to the condition which turns the logic devices off. Consequently, no complete conduction path can exist between the power supply and ground in this precharged state, even if the evaluation device is removed. The gates driven directly from the state flip-flops, however, do not necessarily have their logic devices turned off; consequently, evaluation devices are required for these stages in order to achieve near zero stand-by power. In principle, a string of clocked gates of alternating types can be precharged during the stand-by period; the precharge clocks can be removed; the evaluation signals can be applied to the state flip-flop driven stages; logic signals can then propagate through the string in a ripple-through manner limited only by the transition times of the individual stages.

#### B. Observations

Timing signals are required for the precharge (stand-by) phase, the logic evaluation phase, and the latch enable phase. No additional timing clocks are required -- unlike the case of clocked, non-ratioed, single-polarity circuitry with multiple logic phases. The ideal timing could be achieved with a single system clock. For example, the system clock could represent the stand-by phase when the clock is low; when the clock goes high, the evaluation phase begins and continues until the clock returns to the low state which enables the flip-flops (edge triggered). Dynamic information is used during the evaluation phase; consequently, there is an upper limit on the pulse width for the system clock of about 1 msec.

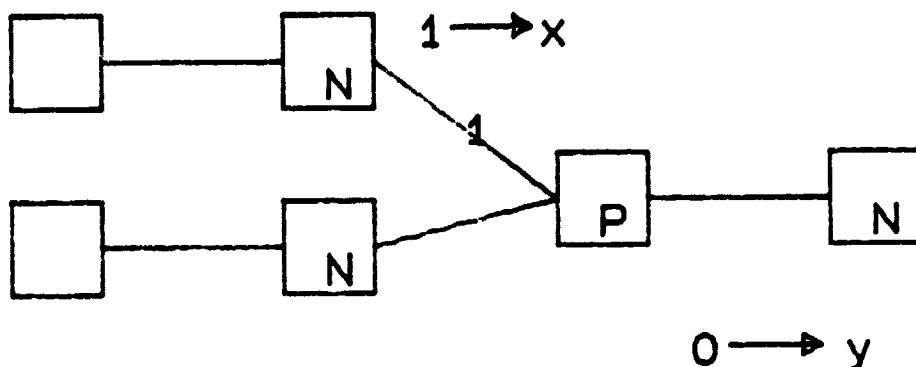
The propagation delay for the ripple-through clocked CMOS should be faster than for classical CMOS or clocked single-polarity circuitry. The discharge delays are achieved through common-source configured FETs, the fastest type, with only single transistor loading per fan-out. Each transition delay begins when the input signal reaches the device threshold instead of the circuit threshold of ratioed or classical CMOS circuitry. There is no added delay associated with additional evaluation clocks as in the case of single-polarity clocked non-ratioed circuitry.

Classical CMOS gates or static gates can be used in place of clocked gates; however, the precharged levels must be compatible as before. This may be beneficial since the

## observations

static circuits can be introduced, however the precharged stages must be compatible. (low stand-by power)

-example



the p-gate could be static

its inputs are precharged high by the n-gate outputs

its output will be precharged low

its output can only drive n-gates

adding extra clocks provides more flexibility at the sacrifice in asynchronous behavior

FIGURE-2 CLOCKED CMOS OBSERVATIONS

classic gate supplies active drive from both directions, although compromising input loading.

It should be noted that the output of any stage can drive any "downstream" stage of the opposite type. As an example, let the first stage from the flip-flops be stage 1 and of N-Type. The P-Gates then fall on the even number of stages and any of them can be driven from stage 1.

Extra evaluation clocks can be added for more flexibility although asynchronous behavior is sacrificed. The added flexibility may be desired in order to achieve a more general form of logic function. Driving an N-Gate with another N-Gate is an example. This subject is dealt with in more detail in the section implementing the PLA logic function.

Figure 3 illustrates a ripple realization of the AND-OR function needed in PLAs. The first stages are N-Gates, series NMOS to provide the NAND function. The second stages are P-Gates, paralleled PMOS also to provide the NAND. The NAND-NAND is one implementation of the AND-OR. The output of the second stage is precharged low and conditionally charged high during the evaluation phase.

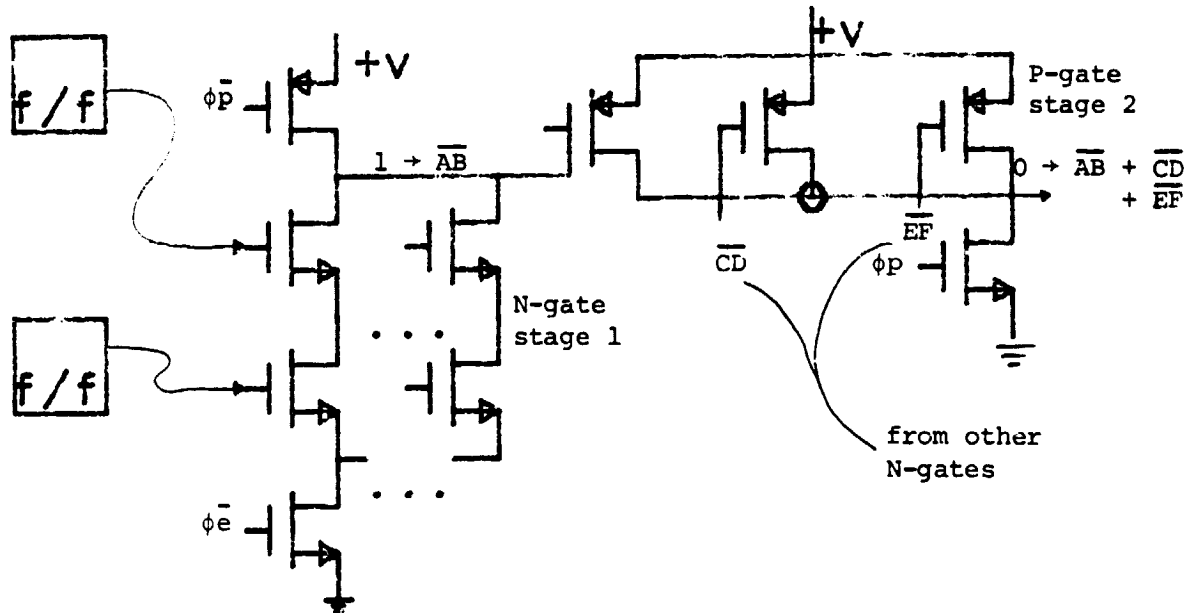
One notes that an entire NAND-OR function can be implemented in the first N-Gate stage by paralleling (providing the OR function) additional discharge paths to ground through series devices (providing the AND function). A consequence of this two-level gate is that the implicants (the AND terms) cannot be shared with other OR gates. Another consideration is the comparative delay associated with series-connected gates having extended fan-in (F/I). Large PLAs require large F/I and, preferably, the implicants can be shared. As a consequence, parallel configured gates are explored next.

#### C. Basic Types of Parallel-Connected CMOS Gates

Figure 4 illustrates five different versions of clocked CMOS gates which utilize parallel connected NMOS logic devices. The classic CMOS gate is also included for illustrative purposes. There are two families of clocked CMOS: the ripple variety without the evaluation device and the gated variety which responses to an evaluation signal. Dual versions exist in the P-Gate type, providing a total of ten versions of clocked CMOS gates using parallel-connected logic devices.

The first of the ripple varieties utilizes common-source logic devices and is labeled NR1 which indicates N-Gate, Ripple, and inverting output. Assuming the N-Gate type, the logic function is NOR; the inputs are precharged low; and the outputs are precharged high. This gate implementation provides the fastest response of all

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the evaluation device in the p-gate can be removed

-if all of the inputs are precharged high by n-gates

the logic gates 'downstream' can only discharge in one direction

there cannot be a race condition

logic decisions are propagated asynchronously during the evaluation time  
can drive the p-gate but  
-an evaluation device is required

the n-gate at stage 1 can drive p-gates at stages 2, 4, 6, etc.

observe: the series n-gate, nand function; the parallel p-gate, nand  
function.

a parallel-series combination at one stage also provides and-or functions

FIGURE-3 AND-OR WITH RIPPLE CMOS

# basic types of CMOS gates (with parallel n logic devices)

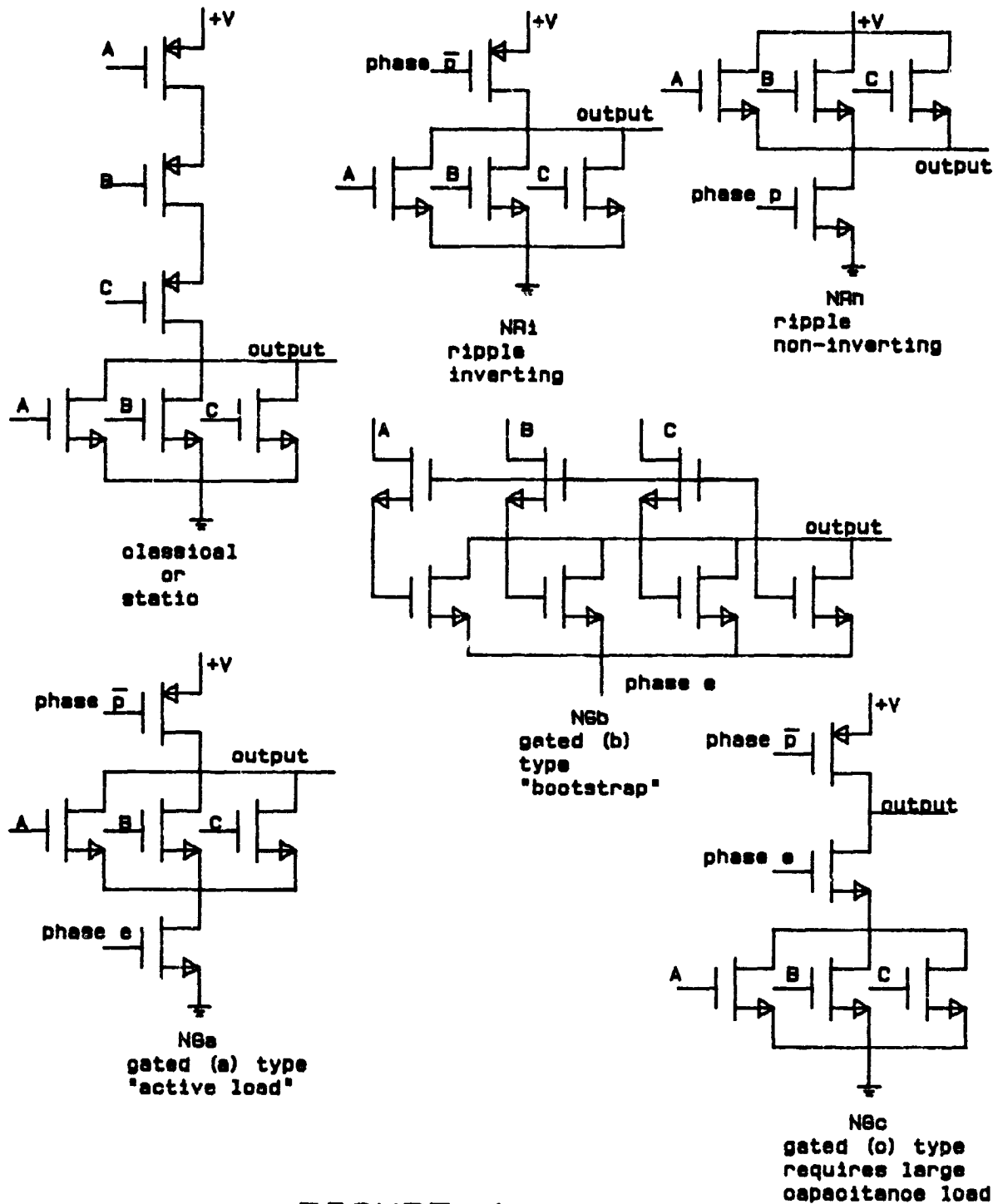


FIGURE-4

the versions.

The second of the ripple varieties utilizes source-follower configured logic devices, which results in a non-inverted output, and is labeled NRn. For the N-Gate the input and outputs are precharged low; the logic function is OR. Since the output voltage swing is not all the way to the supply potential -- limited by a threshold voltage below the rail -- this version is generally not useful and only used in special circumstances. Since the body-effect on the threshold voltage lowers even further the output swing, this version is especially dubious for the logic devices fabricated in "wells", such as NMOS in a P-well process. This variety is approximately an order of magnitude slower than the inverting version -- even to reach its limited output swing. As an example, for a P-well process and with a 5 volt supply, the output swing is approximately from ground to 2.5 - 3 volts. Requiring the output to swing only over a limited range, near ground for the N-Gate, improves its usefulness.

The first and third of the gated versions utilize common-source devices and provide the NOR logic function. Both provide full rail-to-rail signal swings; the outputs are precharged high; and the inputs need not be precharged. The difference between the two relates to the location of the evaluation device.

The label for the NGa version refers to the Gated variety and the fact that its inputs must be driven from an "active" sourcing output to prevent charge splitting. For example, as illustrated in Figure 5, the outputs driving this gate must be able to supply current from the positive supply for a "1" input when the evaluation device is turned on. During precharge the output of the NGa gate is precharged high. One input is presumed to be precharged high, resulting in the (common) sources of the logic devices being precharged high to within one threshold below the supply voltage. The channel is only weakly induced in this case. When the evaluation device is turned on, the source node is pulled to ground with coupling through the full gate capacitance to the input nodes. NOTE that if there is no active source for charging this coupling capacitance, then the input signal level is pulled toward ground, reducing the effective drive of the input. The amount of this signal loss depends on the effective node capacitance of the input and the coupling capacitance of the gate. A precharged output for a simple inverter with a large fan-out requirement would lose significant signal. A classic inverter or a P-Gate can supply the necessary current to provide the full input drive voltage. One also notes that the evaluation device can be shared with other NGa gates.

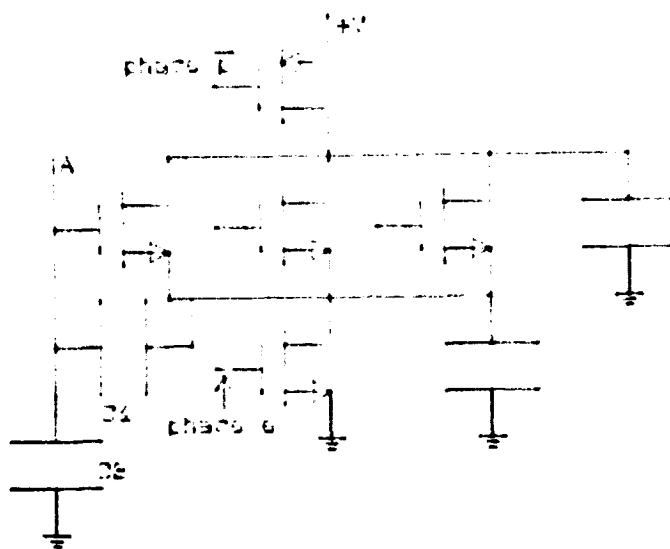
The third version of the gated variety, the NGc



version, has its evaluation device between the output node and the common drains of the logic devices. The "c" refers to the output requirement of driving a large capacitance load when the fan-in is large to minimize charge splitting. When the precharge phase is present, the output is precharged high and the common drains of the logic devices are presumed to be discharged low. If the inputs are subsequently discharged to ground and then the evaluation device is turned on, only the output capacitance is available to supply charge in order to charge the common drain node. The resulting charge splitting may reduce the output signal to unacceptable levels. For example, if the output is driving a simple inverter (minimum fan-out) and the fan-in is large, then the effective capacitance on the common drain node may well dominate the load capacitance, leading to effectively no "1" output.

Another version of the gated varieties of clocked gates is labeled NCB for "bootstrap" from the nature of the circuit action. The sources are tied to the evaluation clock which is at ground during precharge. The drains of the logic and load devices are connected to the output. Since the precharge clock is high during precharge, the output is discharged low during precharge through the load. The input signals are fed through the series devices during precharge to the gates of the logic devices. At the end of the precharge phase the series sampling devices are turned off, leaving the logic device gates charged to some state. If all of the inputs are low, then no channel exists between the evaluation clock and the output; consequently, very little coupling exists between the evaluation clock and the logic gates. When the evaluation clock goes high, the output remains low, at ground. On the other hand, if any one of the gates is charged when the evaluation clock goes high, there is a strong coupling between the evaluation clock and the input through the gate capacitance which bootstraps the gate up with the rising evaluation clock. The channel of the high input remains fully conductive, and sources current from the evaluation clock to the output to charge it high -- even to the supply voltage. If any one of the inputs is sampled high prior to the evaluation clock, the output is subsequently driven high, generating the OR function. The input sampling devices provide isolation between the charged gates of the logic devices and the outputs of the previous stages; however, they may constitute an unacceptable addition to the circuitry. If they are deleted and the inputs are driven from PMOS devices, then the bootstrap action drives the drain junction of the PMOS into forward bias with its associated injection of holes -- a sure method to lead to SCR action and latch-up. Consequently, this version of gated CMOS is likely to have limited utility in bulk

# clocked once circuits

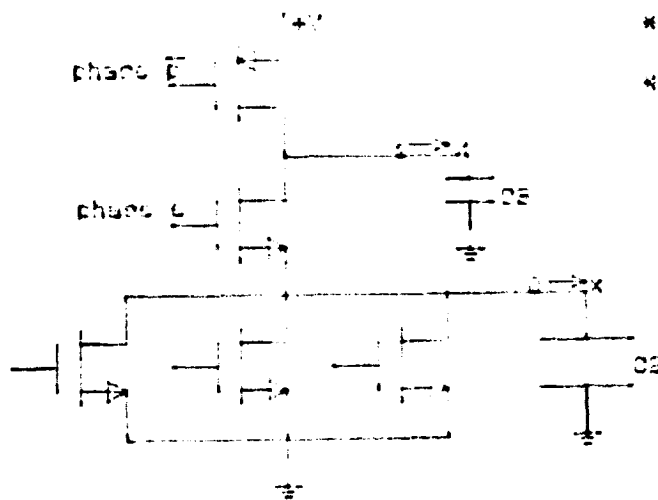


\* sensitive to charge splitting  
if not driven from active source

\* evaluation series can be shared

note that the functional block  
circuit in hand is version of  
this with the evaluation se-  
ries shared

Type (a) "active input"



\* sensitive to charge splitting,  
if  $C_2$  is not  $\gg C_1$

\* a large fan-in implies  $C_1$  to be large

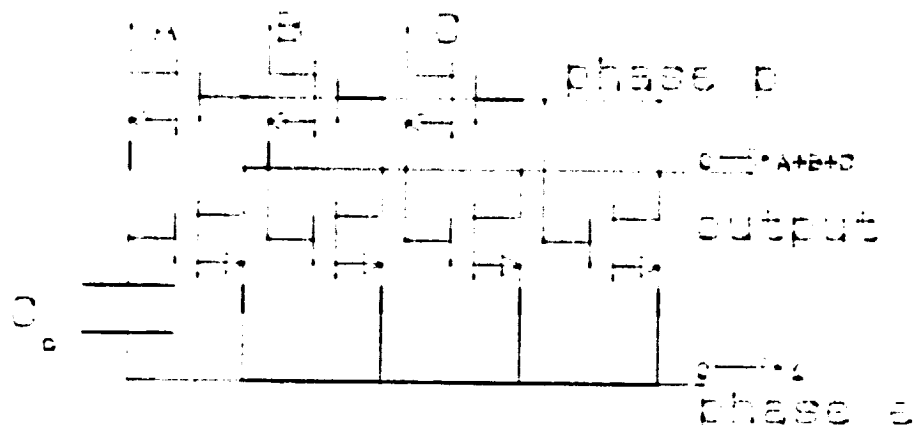
$C_2$  is often a simple input stage

Type (b)  
requires large capacitance load

FIGURE-5 CHARGE SPLITTING CONCERNS

clocked cmos gate

bootstrap



During precharge

phase a=0

output discharged low thru phase a

input signals transferred to the logic device gates

The transfer devices are turned off after precharge

Phase a-- high for evaluation

if all of the inputs were low, there is little capacitance coupling  $C_c$  to the storage node

if one of the inputs is high a channel is formed and  $C_c$  is large the output is driven high with bootstrap action

"or" function for n-gate

"and" function for p-gate

Concerns

if the n-type transfer device is not used and a pmos is used in the storage circuit, then the pmos drain diode is driven into forward bias with bootstrap action.

the result is latch up--

unless one of the following

- 1.) use nmos transfer gate
- 2.) use substrate bias or
- 3.) use SCR or equivalent

FIGURE 6 - CLOCKED CMOS GATE

processes. The methods to provide isolation to prevent latch-up, e.g., substrate bias or the inclusion of the series sampling devices, are likely to result in an impractical gate implementation. For fundamentally isolated structures such as SOS or laser annealed poly over oxide, the bootstrap gate offers future consideration because of its non-inverting logic functions with reasonable speed.

With these possible candidates for logic gates the question remains: Which of the many forms represents the best implementation for PLAs using the CMOS technology?

### III. Programmable Logic Arrays

#### A. The PLA General Function

The typical block diagram of a PLA implemented in NMOS is presented in Figure 7. Latches with sampling at phase 1 provide the complimentary signals and temporary storage during the evaluation period. The AND plane, as illustrated, consist of ratioed NMOS in NOR gate form. The OR plane consist also of ratioed NOR gates. One notes that complimentary signals are used as inputs and outputs. The output of the OR plane feeds the output inverting buffers (latches) which are enabled with phase 2. Since ratioed logic is used, the evaluation period overlaps phase 1 and phase 2.

#### B. Clocked CMOS PLA Timing Concept

A master clock is hypothesized which controls four events, although other clocks may be required and derived from the master.

- 1) Static CMOS latches are used with data clocked in at the trailing edge of the master clock.
- 2) The PLA is precharged in the stand-by state (clock low) to facilitate fast logic evaluation.
- 3) At the rising edge of the master clock the "state" and control inputs are gated into the PLA.
- 4) The signals "ripple" through the AND-OR planes while the clock is high.

Another important assumption is that the fan-in requirements are large which implies parallel gates.

#### C. Ripple AND-OR Planes with Parallel Devices

Figure 8 illustrates the sixteen possible basic functional combinations which provide the equivalent AND-OR function. The task is to select from the possible twenty

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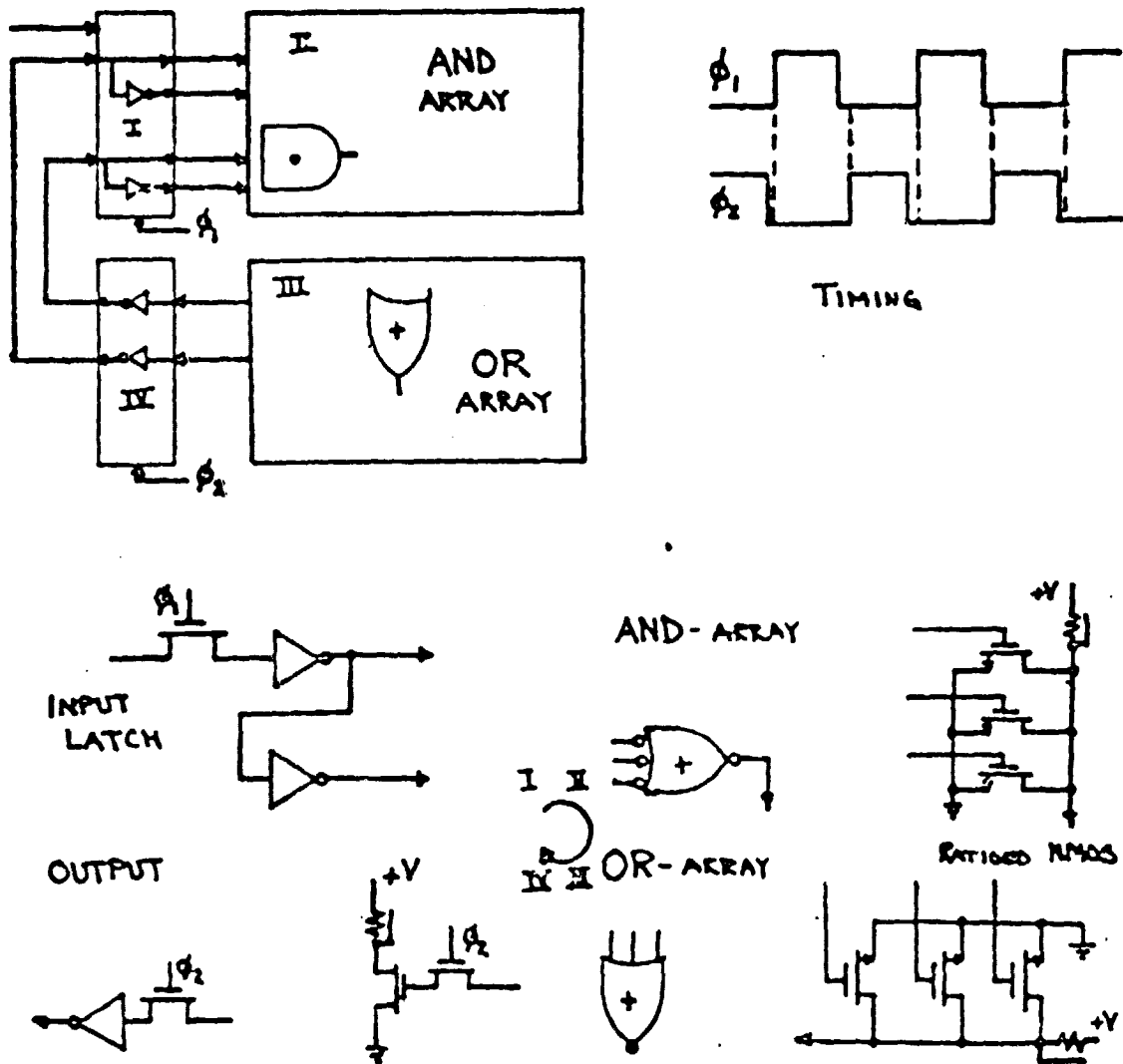


FIGURE 7 - PLA USING NMOS

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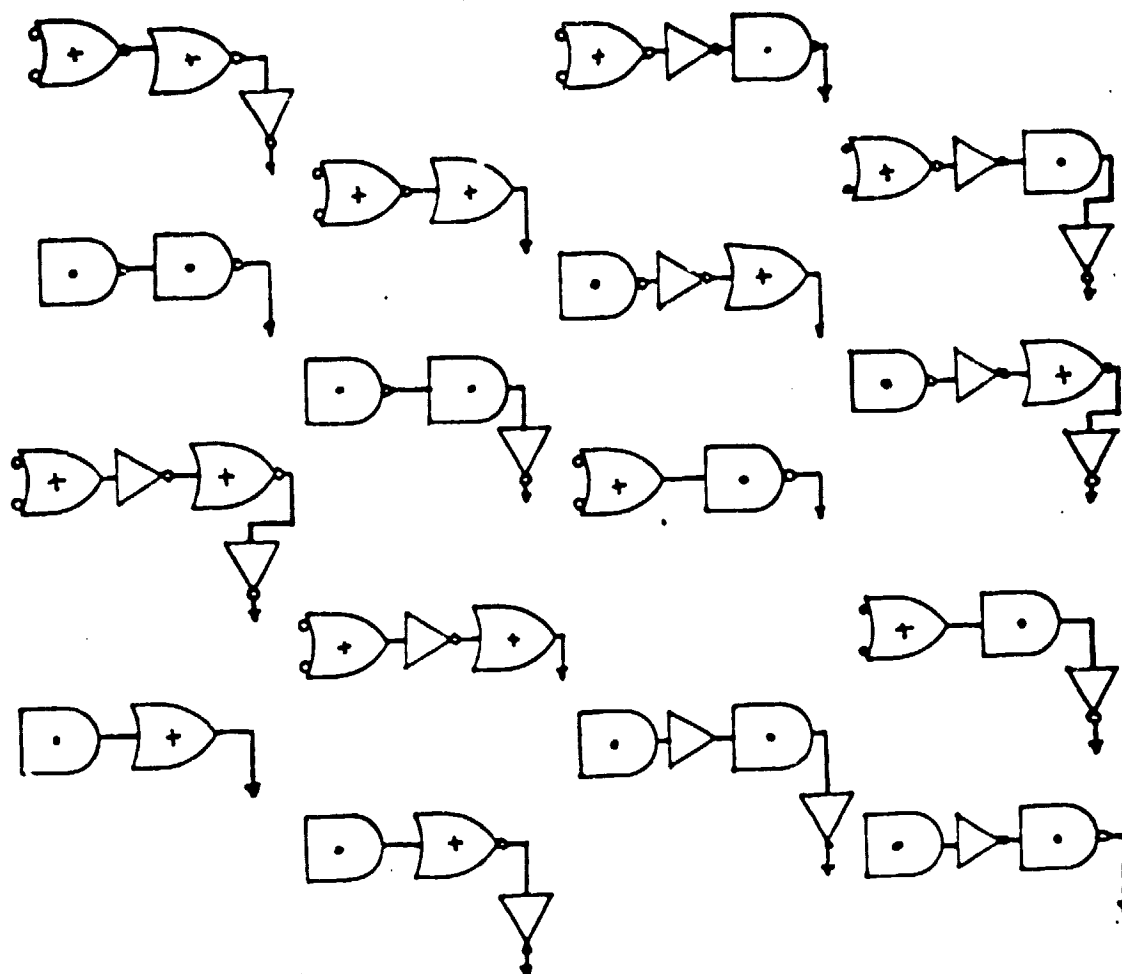


FIGURE 8 - AND/OR COMBINATIONS

clocked, parallel CMOS gates which can be used in these sixteen basic functional combinations. The OR plane is assumed to be of the ripple variety; what are the possibilities? Without regard to the polarity of the output, which can be handled in the latches, four basic combinations are possible:

- 1) NOR    2) OR    3) NOT-NAND    4) NOT-AND

From the ripple versions for these functions one observes that all require that their inputs be precharge low and conditionally charged high during evaluation. How can the AND plane be implemented from either the gated or ripple varieties? This time the polarity of the inputs are of no concern. One finds the following possibilities:

- 1) NAND-NOT    2) AND    3) NOR    4) OR-NOT

One observes that all "AND" outputs must be precharged high and then be conditionally discharged low in contradiction to the OR plane input requirements. The assumed objectives are not possible.

It should be no surprise that the same conclusion is reached if an OR-AND function is sought. All possible outputs for the OR plane are required to be precharged low -- in contradiction to the possible inputs for the AND plane. Hence, the conclusion is that no possible configuration of parallel devices can be realized in a non-ratioed ripple-through form. The alternatives are to consider:

- 1) Series forms    2) Ratioed forms    3) Gating the OR plane

The last appears to best satisfy the requirements of high performance for large arrays at low power.

#### D. Gated AND-OR with Parallel Devices

Of the sixteen possible combinations twelve can be eliminated if the bootstrap gates are disallowed due to latch-up and the source-follower configurations are disallowed due to speed arguments. The four remaining follow:

- 1) NAND-NOT-NOT-NAND    2) NOR-NOR  
3) NAND-NOT-NOR    4) NOR-NOT-NAND

The first has too many levels of logic to be practical. The NOR-NOR version will result in unacceptable charge splitting. Consider that the OR plane is lightly loaded

since it drives simply latches. This implies that the OR plane NOR must not be of the NCo version. The remaining version NCa requires an active source from the previous stage, not achievable with clocked N-Gates. As a result only the last two combinations need further consideration. One notes that the candidates are really the AOI and OAI functions, the duals of each other. This duality allows one to develop a design in either version and translate that design into the other by using the duality principle. One also observes that each contains a NMOS plane and a PMOS plane.

Consider the NAND-NOT-NOR version for further study. The second level of gating can occur at either the inverter or the N-Gate. Both gates which make up the logic planes are driving minimum capacitance and have large fan-in, thus requiring the "a" gate versions. The resulting choices are then reduced to the following:

- (1) (PCa or PRi)-(classic inverter)-NCa
- (2) (PCa or PRi)-PCo-NRi

The gated inverter in the second version is assumed to be limited to the "o" version because no active drive is available from the previous stage. The PCo gate requires a large output load capacitance. If this is not the case in the minimum fan-out of one, then unacceptable charge splitting may result. Possibly in some designs the resulting charge splitting is less using the PCa inverter since the output of the first stage is likely to have a high output capacitance. These compromises in charge splitting relative to particular designs and programming lead to the conclusion that the classic inverter is a far safer approach in spite of its possibly slower performance. For this reason the classic inverter approach has been selected for this design effort. Figure 9 illustrates this approach schematically.

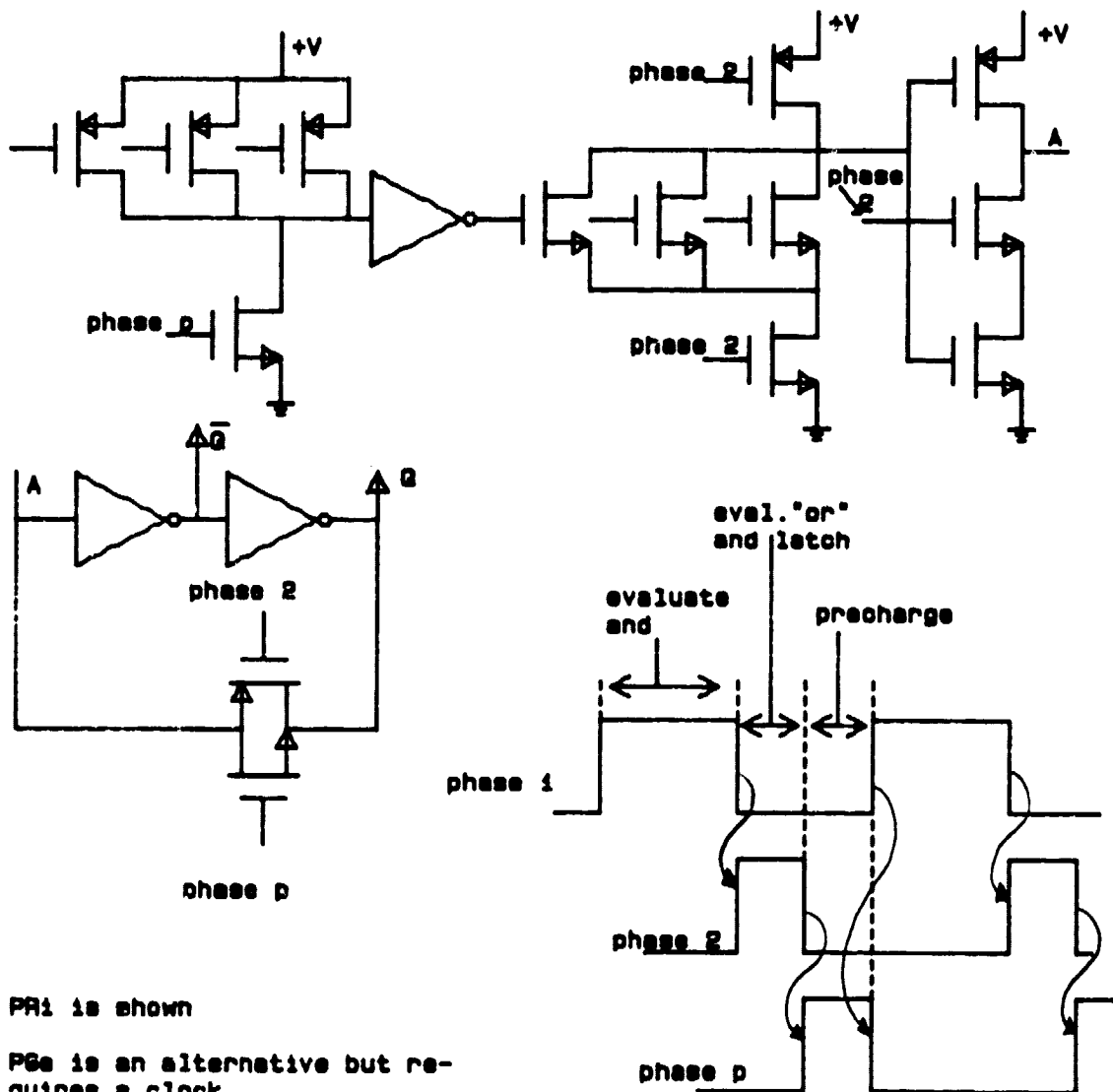
#### E. Input Partitioning

ANDing together two signals before entering the AND plane is sometimes used as a means of compacting the design. This partitioning is considered as a programming option. The inputs to the PLA are assumed to run globally around the chip and be subject to noise. Adding a buffer inverter improves the signal level for sampling which occurs during the precharge state. The information is stored as charge on capacitance (gate) during the evaluation state. Double inverters provide the necessary active drive for the true and compliment signals. The input partitioning can be achieved with NOR gates implemented as NCa versions which supply the evaluation



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# dynamic cmos PLA (based on N2a "or" array)



PR1 is shown

PGa is an alternative but requires a clock

NRn requires a second array of nmos transistors and is usually slower than the above. this is especially true for p-well processing

FIGURE-9

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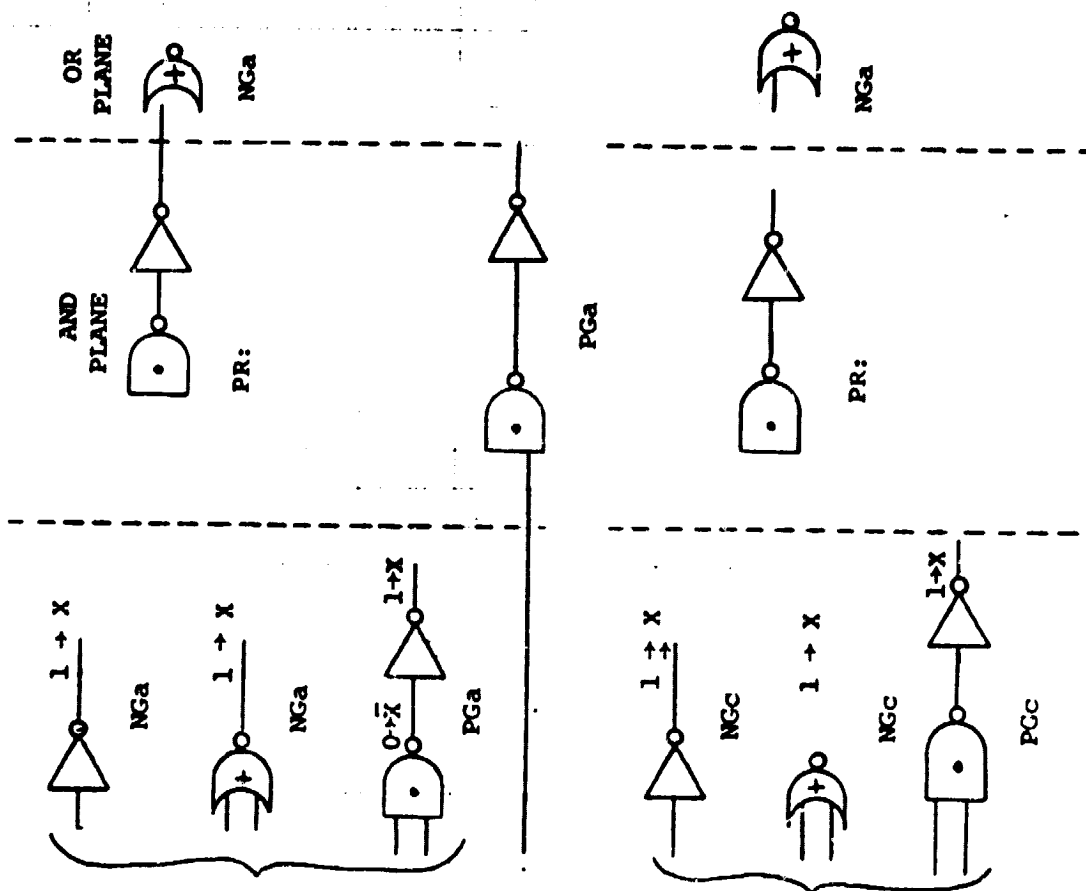
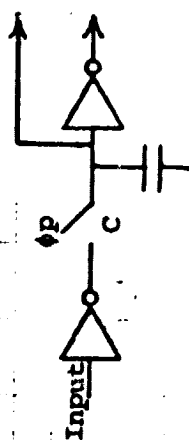
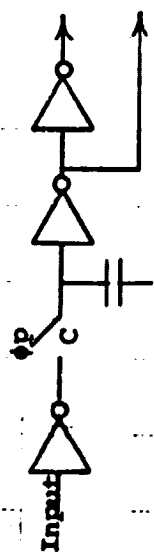


FIGURE 10 - ALTERNATE INPUT CIRCUITS



CHECK: Charge Splitting

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gating for the AND plane of the PLA. The AND plane can then be implemented with ripple gates PRI for higher performance. This approach plus alternates are illustrated in Figure 10. In some designs where the input capacitance to the AND plane is assured to be sufficiently large, NGo gates can be used with the associated elimination of one input inverter.

#### F. Latches

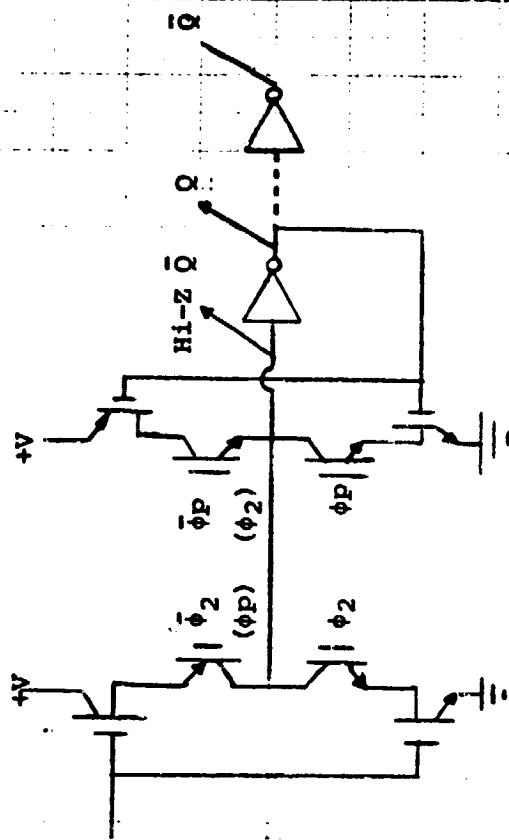
Figure 11 illustrates various versions of latches. The switch notation with a N, P, or C indicates a transmission gate implemented with a NMOS transistor, a PMOS transistor, or both as in classic CMOS. The classic CMOS transmission gate utilizes the common-source operation for both devices to provide rail to rail coupling whereas the single polarity types suffer a threshold drop in signal when coupling as source followers.

The classic NMOS version of a latch is indicated for reference. If the CMOS version is implemented with CMOS transmission gates, active drive in both directions is required as an input. If the input sampling device represents one of several multiplexing switches, then two sampling clocks for each input are required. By adjusting the gain of the first inverter and utilizing only the transistor not fabricated in the "well", one of the complement sampling clocks can be eliminated.

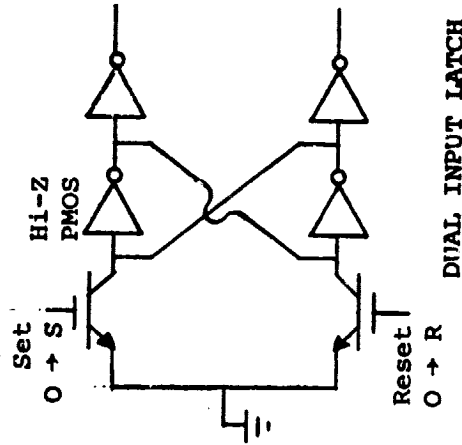
The common CMOS sample-and-hold circuit, sometimes referred to as the "H" latch is also illustrated. This version suffers also in not providing symmetric drive from the two outputs. A major advantage of this type, however, is that the input impedance is only capacitance. The input signal can be charge on this capacitance at the time of enabling the latch unlike the first versions.

A simplified version of the "H" is illustrated which utilizes the fact that the input is precharged high. At phase 2 the input is sampled and enables the latch. The feedback path is illustrated as a high impedance path in order to minimize the clocks required. The drive from the input sampling inverter must over power the feedback in this case. After the signal propagates through the two inverters, the full logic levels are generated with near zero stand-by power achieved. If only temporary storage of information is required, then the feedback is not required at all.

A dual input form of a latch is also shown. This version requires sufficient ratios of the pull-down devices compared with the internal PMOS devices such that the internal latch can be upset. As before, after the input signal has propagated through the internal latch, the logic levels are fully established and near zero stand-by power

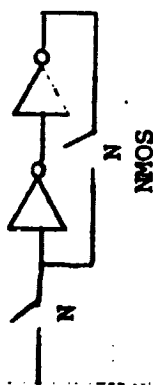


"H" GATE

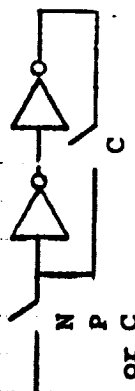


DUAL INPUT LATCH

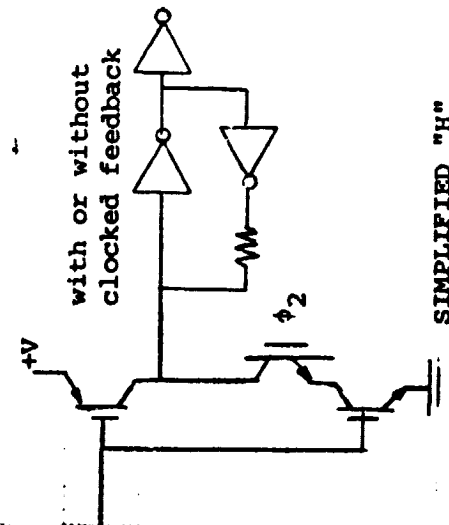
FIGURE 11 - LATCHES



Simple CMOS



Simple CMOS



Simplified "H"

is achieved. Output drive buffers are included to supply adequate source current. There is an advantage of this configuration: since the set and reset transistors are turned off during the precharge (stand-by) state, only a low-to-high signal from the OR plane is required for setting or resetting, without any clock timing signal required for enabling. The disadvantage is that two outputs from the OR plane are required for each flip-flop -- even though these involve less complex functions.

#### G. PLA with Single-Ended Latches

Figure 12 illustrates a clocked CMOS PLA with a single-ended latch. It uses the PRI-classic inverter-NCA version. It also uses an extra clock with which to gate the latch in order to prevent the glitch in the latch output which would occur if the latch is enabled at the same time as the OR plane. Since the outputs are isolated from the PLA inputs during this time by the input sampling devices, not shown, this glitch does not constitute a logic error in the PLA. The system requirements may not allow it, however. If the glitch is not harmful then phase 1' can be merged with phase 2, saving one clock.

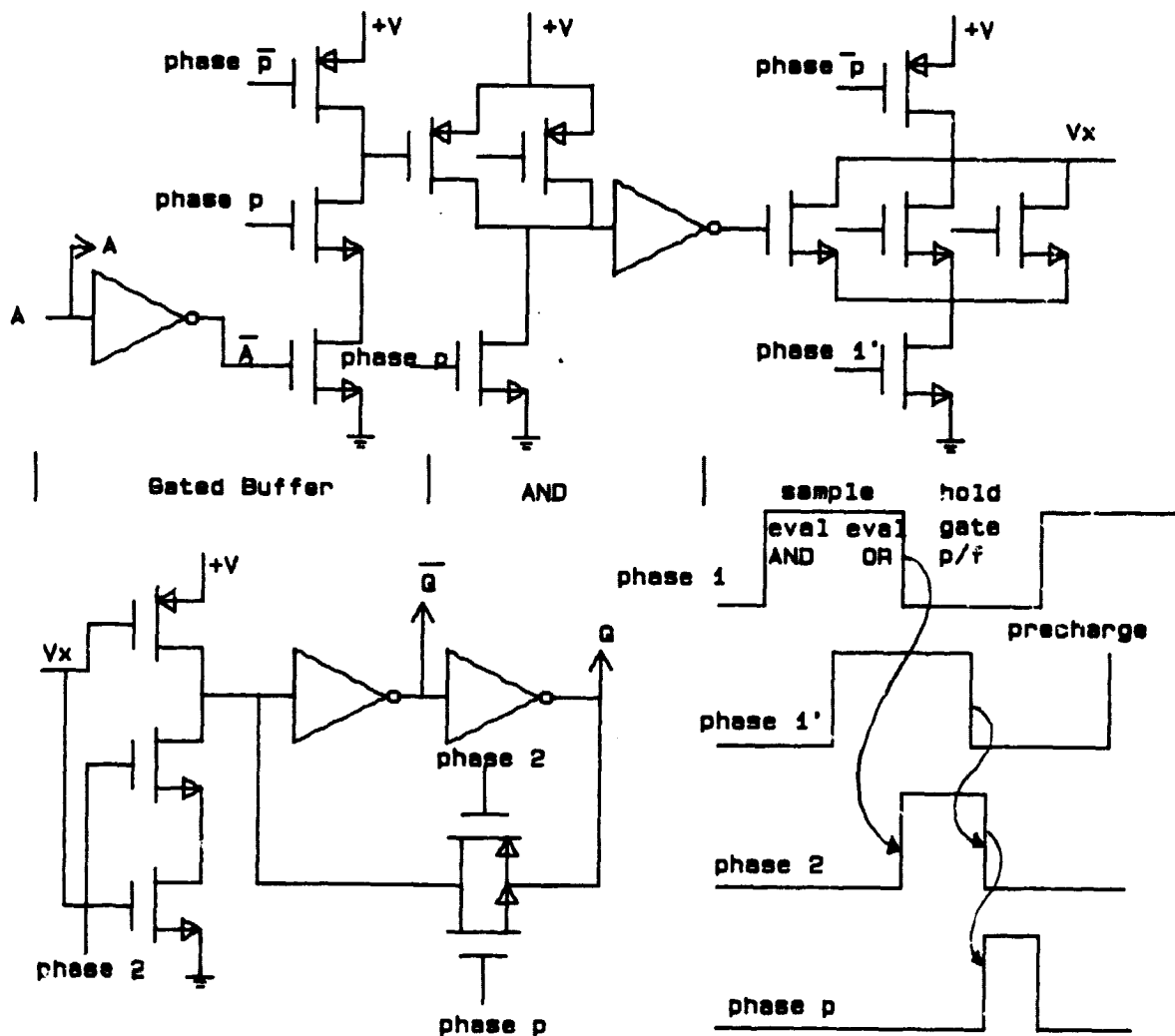
#### H. PLA with Dual Input Latches

Figure 13 illustrates the PLA/SLA with dual input flip-flops. In order to achieve good ratios in the latch the set transistors are selected as NMOS with their inputs precharged low. This requires that their inputs are driven by PCA gates. This implies the dual version of the PLA, i.e., the OR plane is implemented in PMOS, and the AND plane is implemented in NMOS. One additional timing event is required: the beginning of the stand-by or precharge state. A one shot type action is required with the action triggered by the falling edge of the master clock.

#### IV. Star Layouts With Dual Input Latches

Figure 14 illustrates a possible chip floor plan for a SLA using the attached cell designs which are based on a STAR type foundation. The design shows the output buffers around the chip with an interconnection bus routing signals around the chip just outside of the buffers. Internally in the chip is the folded array with the AND plane made up of parallel NMOS devices connected along columns (vertical). The inputs feed in along rows from the outside through the output buffers and the latches to the input circuitry. Along each row two signals with their compliments are routed into the AND plane. The implicants are generated from columns of NMOS devices with their

# DYNAMIC CMOS PLA (with alternate timing for no output glitch)



requires another clock signal

FIGURE-12

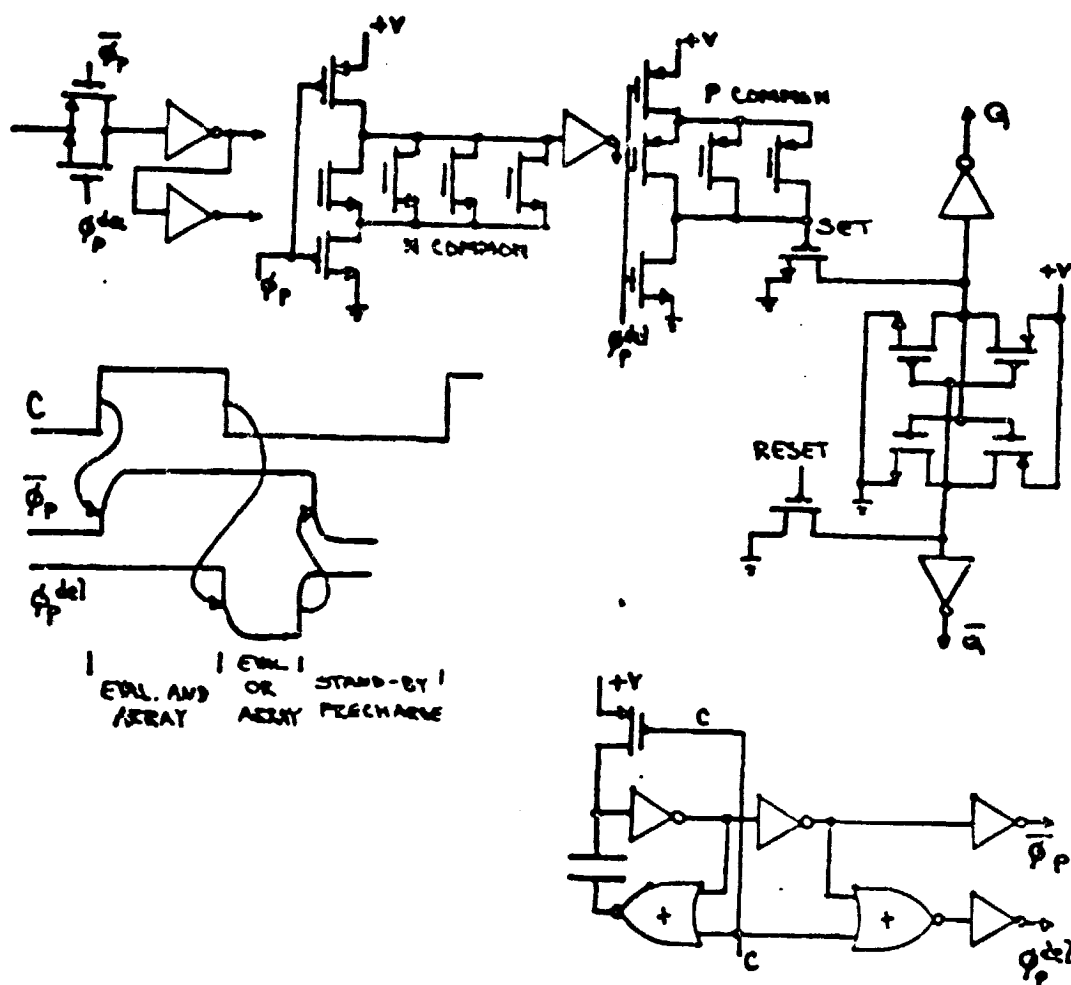
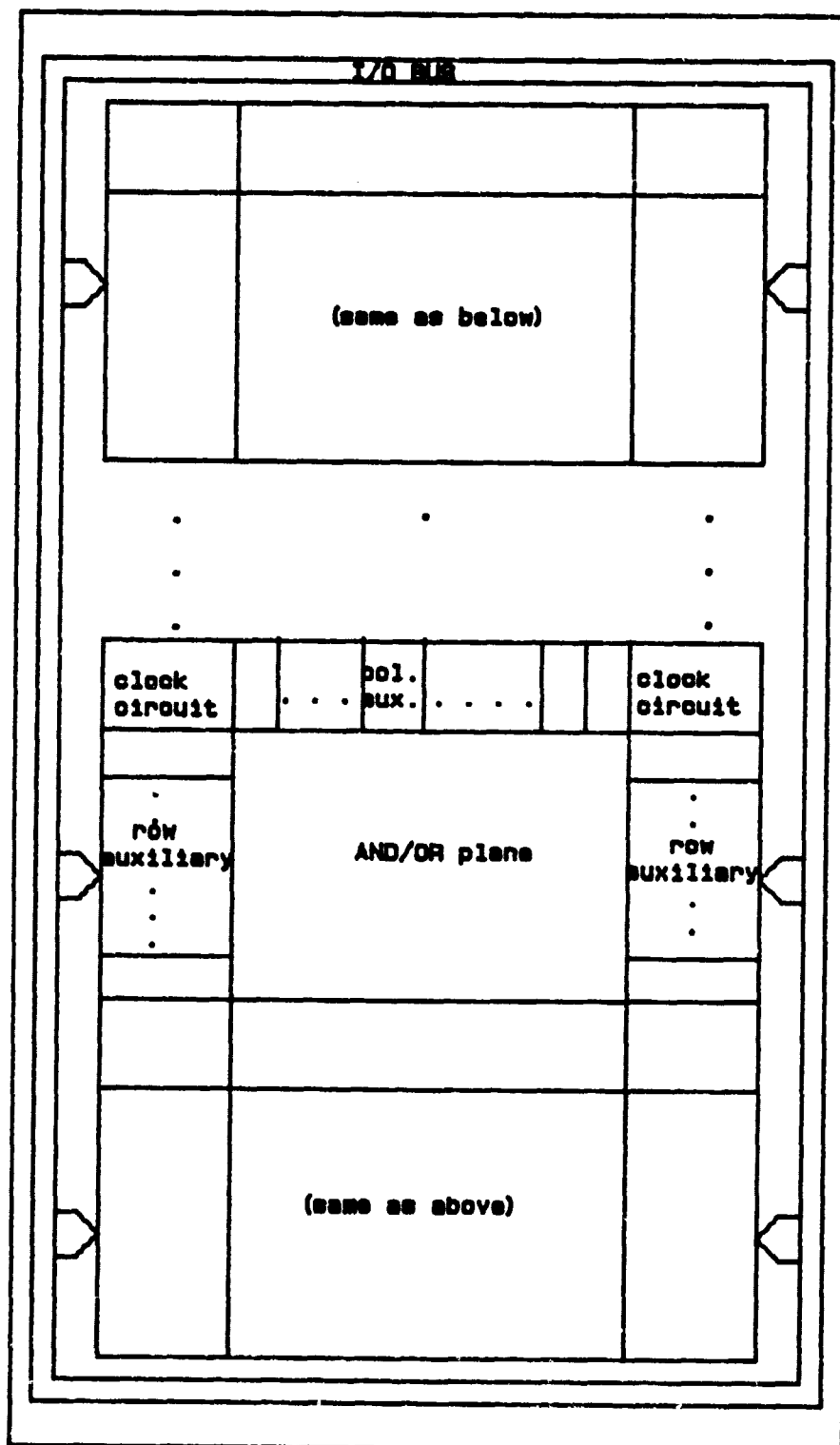


FIGURE 13 - PLA/SLA WITH DUAL INPUT F/F

outputs feeding into two dedicated rows which provide the inverters and the "load" devices for the implicants. The outputs of the inverters are fed back down the column to serve as inputs to the horizontal rows of parallel connected PMOS serving as the OR plane. The outputs of the OR plane run horizontally back to the set and reset transistors of the latches. Miscellaneous row oriented devices are grouped into the NCOM and PCOM cells between the input circuits and the array itself. It should be noted that the actual boundaries of the various gates used in the AND and OR planes can be moved to fit the individual requirements for the logic in question. This is possible since the arrays are back-to-back (merged).

The detailed cell designs are included in the following figures.





CHIP FLOORPLAN

FIGURE-14

# LEGEND



-----	FIRST METAL
-----	SECOND METAL
	TRANSISTOR
	DIFFUSION CONTACT
#	FIRST METAL TO SECOND METAL CONTACT

FIGURE-15

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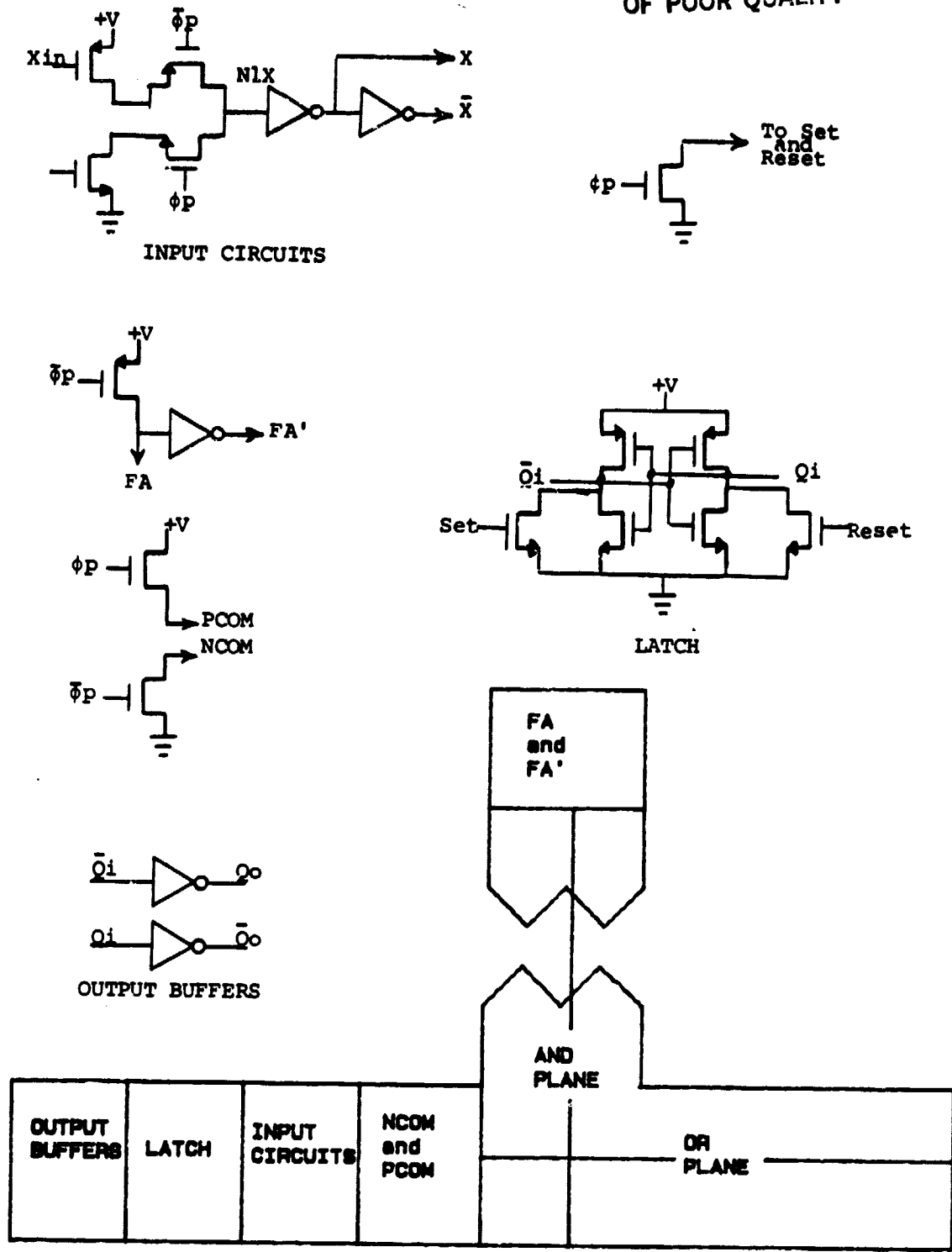


FIGURE 16 - CHIP FLOORPLAN DETAIL

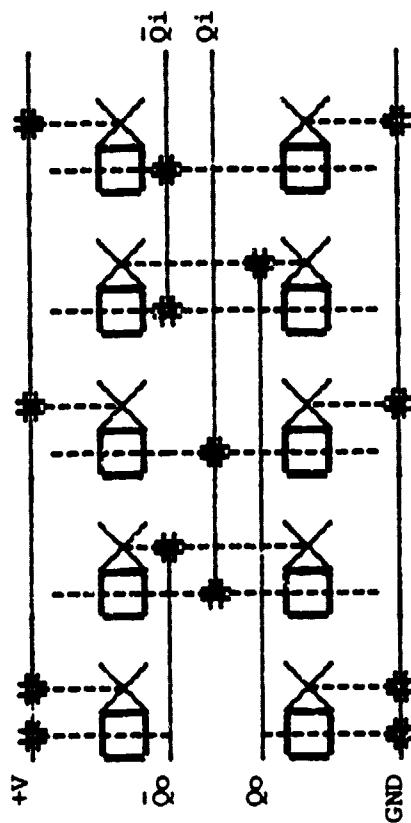


FIGURE 17 - OUTPUT BUFFER CIRCUIT DETAIL

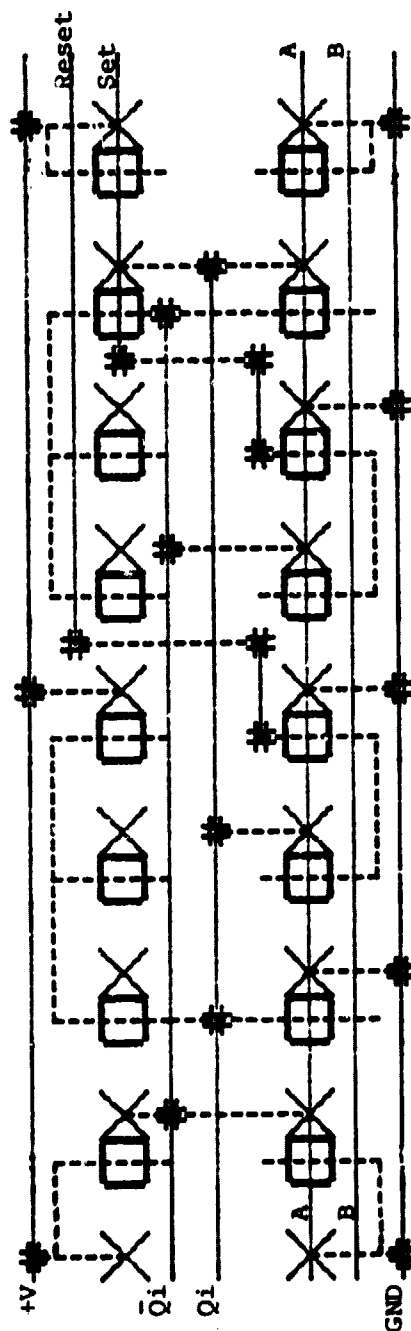
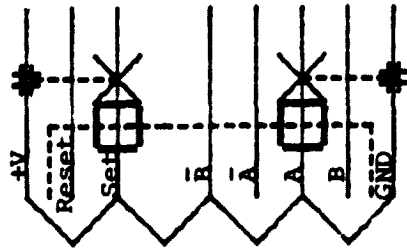


FIGURE 18 - LATCH CIRCUIT DETAIL



INSERT  
FIGURE 20

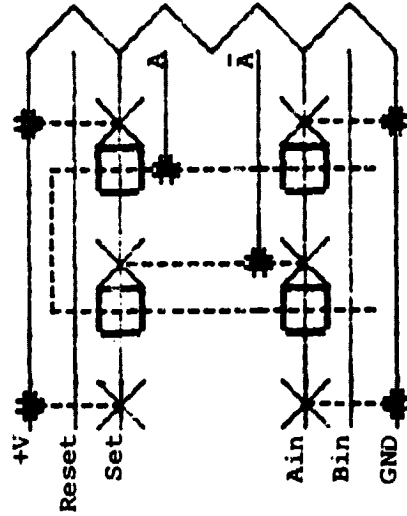


FIGURE 19 - INPUT CIRCUIT DETAIL

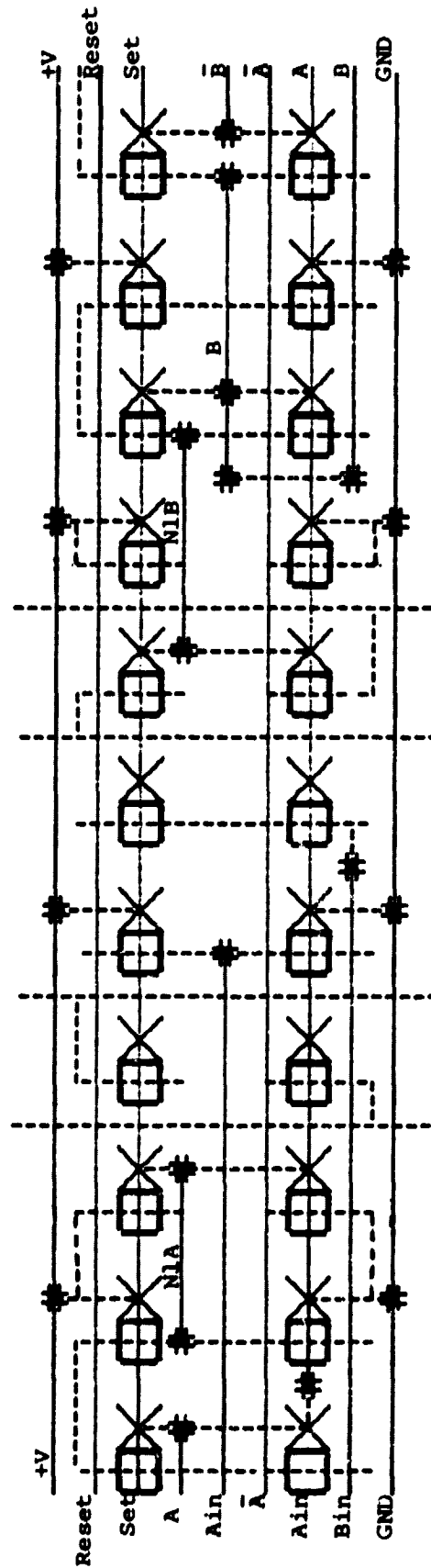


FIGURE 20 - INPUT CIRCUIT DETAIL

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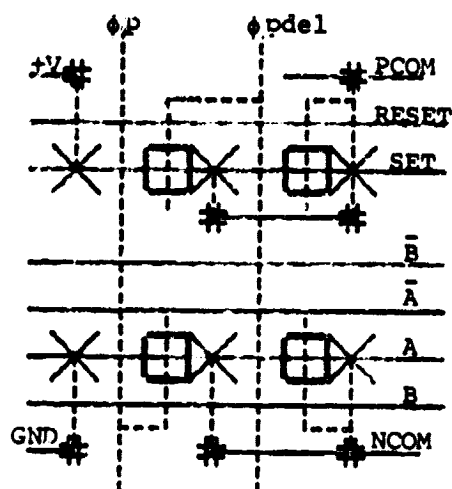


FIGURE 21 - NCOM AND PCOM

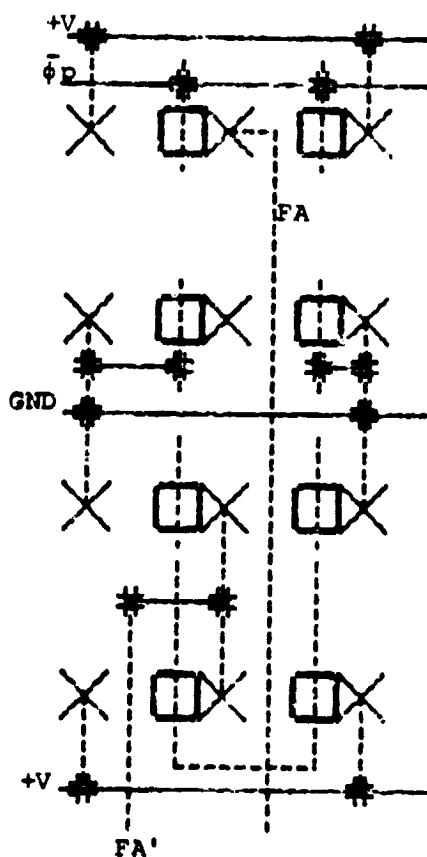


FIGURE 22 - FA AND FA'

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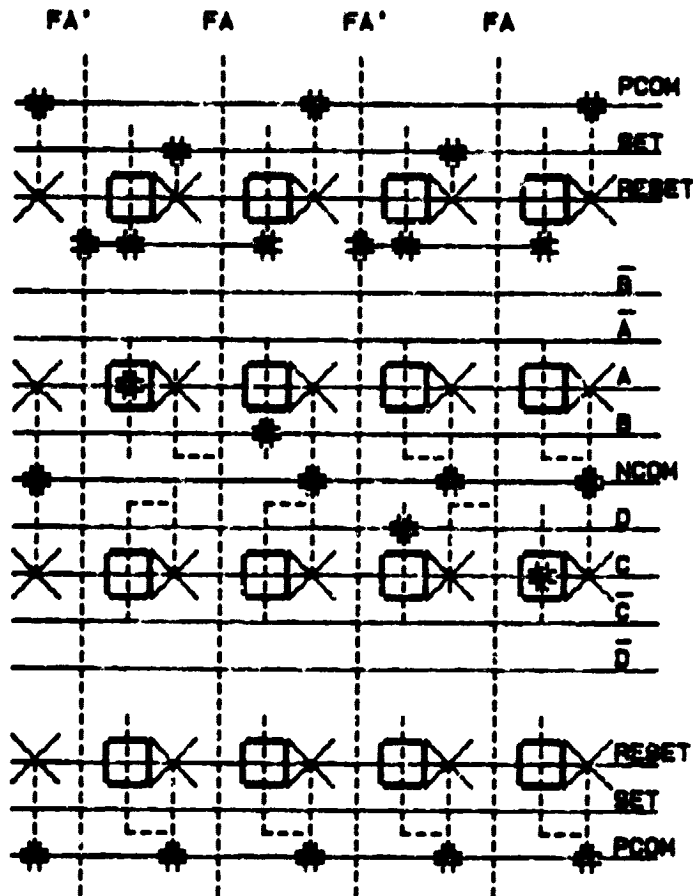


FIGURE 23 - AND/OR PLANE DETAIL

## REFERENCES

1. S. S. Patil and T. A. Welch, "A Programmable Logic Approach for VLSI", IEEE Transactions on Computers, Vol. C-28, No. 9, September 1979, pp. 594-601.
2. R. A. Wood, "A High Density Programmable Logic Array Chip", IEEE Transactions on Computers, Vol. C-28, No. 9, September 1979, pp. 602-608.



**END**

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